CIMdata

PLM Industry Summary

Christine Bennett, Editor

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CIMdata News

"2008 PLM Market Growth Was Strong Going into the Global Economic Downturn" by Ed Miller

30 June 2009

According to recent statistics compiled by CIMdata, the Comprehensive PLM market experienced a

6.7% growth in 2008 with all sectors showing increases. Surprisingly, these increases fell only slightly short of earlier expectations, primarily because of a robust start for PLM investments in the first half of the year. Only in the last quarter did the market slow appreciably, which will undoubtedly continue in 2009 until the economy turns around. Nevertheless, a wide range of companies are investing in PLM to achieve short-term benefits as well as long-term strategic value throughout the product lifecycle and across their extended enterprise. Indeed, PLM may be one of the major deciding factors in determining which companies are able to weather the current economic storm and be in the best competitive position when global markets rebound.

Business Survival and Long-Term Priorities

Investments and implementation of PLM are being driven on several fronts. Small and mid-size companies continue to deploy PLM, as well as both new and expanded solutions at some of the world's largest enterprises. Moreover, a widening range of industries are utilizing PLM including both traditional industries such as automotive, high-tech electronics, and aerospace and defense, as well as companies that have not historically been major PLM investors, such as food and beverage, retail and apparel, financial and investment services, and government. In addition, a renewed focus on PLM is taking place in areas such as utilities, petrochemical, construction and infrastructure.

In the current economic climate, many companies are primarily focused on the bottom-line benefits of PLM for controlling costs and improving operational efficiencies. The emphasis at these organizations is toward quick value, bite-size investments that will provide the fastest impact. Indeed, CIMdata research of companies that have implemented PLM solutions indicates that typical ROIs can be substantial and contribute heavily toward whether the company is able to effectively compete and even survive in today's economy.

Even as these short-term priorities dominate the current market, long-term strategies still continue at many companies focusing on using PLM to best position themselves competitively for when the world emerges from the current economic chaos. Long-term drivers for PLM continue to be focused on initiatives that are critical for business success, including the harmonizing of global processes, managing the increased complexity of products and value chains, and improving competitiveness and pricing structures by improving product quality and lowering costs.

As a strategic enterprise investment, PLM is rapidly extending beyond engineering design to a broader range of business functions—from early-stage product strategy development and planning, to product engineering and manufacturing engineering, and through to product maintenance and support. The impact of the PLM footprint expansion is that many diverse, previously-isolated disciplines and pockets of automation are now being tightly integrated and efficiently coordinated through comprehensive PLM solutions. These solutions allow the various groups to collaborate more effectively and work more efficiently, leveraging corporate-wide product knowledge.

The Value of PLM in a Dismal Economy

CIMdata defines PLM as not just a set of technologies, but a strategic business approach that applies a consistent set of business solutions in support of the collaborative creation, management, dissemination, and use of product definition information across the extended enterprise from concept to end of life—integrating people, processes, business systems, and information. In this way, PLM forms the product information backbone for a company and its extended enterprise.

The tremendous business value in such an integrated, end-to-end environment is that processes are optimized not for individual departments or groups, but for the entire enterprise and across the full

product lifecycle—planning products that fit into the company's business, and developing product designs that meet those plans and that can be effectively built, sold, and supported. With that broad view and overall optimization of processes, companies operate more efficiently, get to volume production faster, improve quality and product performance, and have the ability to design more innovative products.

Considering the far-reaching corporate business impact of implementing such an expanded PLM strategy, the approach has become a critical enterprise investment. PLM is widely regarded as a necessity in a turbulent global economy where companies leveraging it as part of their corporate strategy will likely be among the top performers in the coming years as the economy improves.

Growth in All Segments of the PLM Market

CIMdata's PLM market analysis provides two perspectives on PLM:

* **Comprehensive PLM** covers the full product definition over the entire product lifecycle, and across all industrial industries. This includes mechanical, electronic, and software components, as well as both discrete and process industries.

* **Mainstream PLM** covers a subset of the Comprehensive PLM market, but includes the subsectors that have traditionally been addressed by the major suppliers (i.e., drivers) of the PLM market.

According to recent statistics compiled by CIMdata, the worldwide Mainstream PLM market experienced 7.8% growth in 2008 to reach an estimated $16.7 billion for software and related services. Mainstream PLM is expected to continue a steady climb over the next five years, increasing at a compound annual growth rate of approximately 4.2% and expanding the market size to over $20 billion by 2013. However, with the continuing impact of the global economic down turn, growth in 2009 is forecast show a very slight decline (-0.2%) versus 2008.

Looking at the broader view of the market, Comprehensive PLM investments grew 6.7% to reach $26 billion in 2008. The boost is attributed to recognition of the enterprise-wide value of PLM in increasing efficiency, lowering costs, and improving quality for companies of all sizes in a growing number of industries—most particularly in light of the continuing global economic downturn. Investments are forecast to achieve a 4% compound annual growth rate through 2013, when market size is expected to reach $31.7 billion. Again, growth for 2009 is forecast to decline slightly (-0.7%).

CIMdata also segments the overall PLM market into three major sub-sectors:

* **Tools** (applications and solutions) that create product-related intellectual assets through authoring (e.g., CAD), analysis, modeling, simulation, and documentation of product and plant/facility information.

* **Collaborative Product Definition management** (cPDm) applications and solutions to capture, manage, disseminate, visualize, and collaborate on product-related intellectual (digital/virtual) information, including related processes.

* **Digital Manufacturing** solutions for process planning, resource definition, factory floor layout, and product flow simulation and analysis—including ergonomics.

According to CIMdata, the Tools sector investments by companies worldwide increased 6.8% in 2008 for a total of $16.9 billion on solutions such as mechanical computer-aided design (MCAD), computer-aided manufacturing (CAM), electronic design automation (EDA), engineering simulation and analysis, architecture/engineering/construction (AEC), technical publishing, and others. The Tools portion of the

PLM market is forecasted to grow at a compound annual growth rate of 3.5% (-1.1% decline is forecast for 2009 versus 2008) over the next five years to reach $20 billion by 2013.

CIMdata statistics indicate that expenditures in the cPDm segment increased 8.9% in 2008 for a total of $8.2 billion for software and services related to PDM, collaboration and visualization, data exchange, portfolio management, compliance management, strategic sourcing, enterprise application integration, workflow, functional applications such as configuration management, and solutions for specific industries or businesses. The cPDm segment is expected to exceed $10.5 billion by 2013 for a compound annual growth rate of 5.1% (flat growth of 0.2% is forecast for 2009).

The Digital Manufacturing segment of PLM increased more than 9% to a total of $530 million in 2008, according to CIMdata statistics. This segment is expected to have a 4% compound annual growth rate over the next five years (-1% growth forecast for 2009) and exceed $650 million by 2013. Because the definition of production processes is a critical part of the product lifecycle and is directly impacted by product designs, Digital Manufacturing is becoming an important element of PLM strategies. Indeed, Digital Manufacturing is a key point of integration between PLM and factory automation equipment such as PLCs and transfer lines, and many of the long-term benefits from PLM are simply not achievable without incorporating a comprehensive Digital Manufacturing strategy.

Leading PLM Solution Providers

While there are many companies participating in the PLM market, a few have distinguished themselves as “PLM Mindshare Leaders.” These companies are typically considered to be at the forefront of the market in terms of either revenue generation or thought leadership.

With broad-based capabilities that support a full product lifecycle-focused solution, these mindshare PLM suppliers all sell some or all of their products and services through their own field sales and support organizations. This is their core or direct revenue. Each also has an increased market presence associated with consultancies, systems integrators, value-added resellers, and other partners that sell and provide services based on the mindshare leaders’ technologies and products. The combined core and partner revenues can greatly expand the visibility and impact of a supplier in the industry, generating a significant market footprint.

Based on these combined revenues, the global PLM market presence (no double-counting of revenues and royalties) for the PLM Mindshare Leaders was determined, with Dassault Systèmes (Dassault) the PLM market presence leader again in 2008. Note that the revenue generated by IBM’s Dassault-based PLM services business is a significant contributor to Dassault’s market presence. Following Dassault were Siemens PLM Software (Siemens), PTC, SAP, and Oracle in that order. They all exhibited strong and growing partner programs in 2008, providing a positive basis for future growth of their overall market presence.

A widely diverse group of suppliers provide solutions and services focused on cPDm, one of the most visible and central sub-sectors of the PLM market. However, the same PLM Mindshare Leaders mentioned previously are also the cPDm market presence and direct revenue leaders. CIMdata’s analysis of cPDm market presence for the market leaders reinforces the impact that partner revenue has on a supplier’s cPDm PLM footprint.

Siemens was again the cPDm market presence leader for 2008, with both significant direct revenues and strong partner revenues from several of its partners. Dassault was second, with IBM generating the significant portion of its partner revenues, followed by SAP, PTC, and Oracle respectively.

The leader in cPDm-only direct revenues for 2008 was SAP, which continues to generate substantial cPDm revenues by selling within its installed base and into industries that have not been traditionally dominated by mechanical design issues. SAP was followed by Siemens, PTC, Dassault, and Oracle. All these vendors had good growth in 2008 as adoption of cPDm solutions as part of enterprise PLM strategies continues to grow, with many of these organizations generating substantial revenues from services.

Five-Year Outlook

Although CIMdata's estimates for PLM market growth in 2009 reflect the impact of the current economic impact, it is expected to have solid growth over the next five years as companies recover from the current recession and continue to invest in solutions that can provide them with sustainable business advantage and profitability. CIMdata expects that the cPDm sector of the PLM market will be the fastest-growing segment as companies invest to better leverage product and plant information across the lifecycle from concept, through manufacturing, to service and operation. In addition, evolution of PLM's definition and scope will continue to fuel growth in both software and services as PLM becomes more important than ever and companies more deeply embedded the approach within the enterprise.

Column from: Time Compression, Contributed by: Ed Miller, President, CIMdata Inc. | e.miller@cimdata.com

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Has Your Company's Situation Changed Regarding Your PLM Program Progress since January of this Year (Opinion Poll Results)

24 July 2009

The results for the last CIMdata opinion poll are:

How has your company's situation changed regarding your PLM program progress since January of this year?

Answers	Votes
Situation is worse, and it has been further delayed or reduced	24%
No change at all	37%
Situation is improving, and it is proceeding with reduced delays	21%
Situation has improved, and it is proceeding without additional delay	18%

Has the direction of your PLM program changed significantly since January of this year?

Answers	Votes
No change in direction	52%
Change in business areas prioritized for support	27%
Change in regions prioritized for support	3%
Change in business processes prioritized for support	6%
Other changes in direction not listed above	12%

CIMdata's latest opinion poll asked if the economy had impacted company PLM programs this year. The results were better than expected. The first concerned the progress of PLM programs. More than a third of respondents (37%) indicated that there had been no change. This indicates that many companies have remained committed to their PLM initiatives and are continuing to acquire and deploy PLM solutions. Another 18% indicated that the situation had improved and their programs were now proceeding without further delays while 21% indicated that their programs were proceeding with some delays. Only 24% indicated that their situation had worsened and their PLM programs were being delayed or reduced in scope. The fact that 75%+ indicated continuing progress reflects management's understanding of the importance of PLM to help a company maintain or improve its competitive position in times of stress and also that PLM can help reduce the overall cost of product development.

The second question asked if companies had changed the direction (focus, scope) of their PLM program. 52% responded that there had been no change in direction while 27% indicated that there had been changes in priorities to focus on supporting specific business areas. The remaining 21% indicated that there had been miscellaneous direction changes. These results would indicate that most companies are following their PLM plan with the confidence that it should provide the support they need. They are evaluating how PLM can best support specific business areas and adjusting their programs to focus on those areas in which they can get the biggest return on investment.

NOTE: The results of these polls are anecdotal, not scientific.

If you have a suggestion for a poll you'd like to see contact us at info@cimdata.com.

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CIMdata in the News "Ways Manufacturers Are Going Green And Don't Even Know It"

21 July 2009

In the article, Ways Manufacturers Are Going Green And Don't Even Know It", published in Manufacturing.net, Patrick Michel, Vice President, DELMIA Industry Solutions & Marketing cites findings from the CIMdata report, The Benefits of Digital Manufacturing, that companies using digital manufacturing can see a 40 percent reduction in manufacturing process planning; 30 percent reduction in lead time-to-market; a 15 percent increase in production throughput; a 13 percent decrease in overall production cost; and a 40 percent reduction in equipment costs" and concludes not only does digital manufacturing serve as the ultimate competitive advantage but it also provides many green benefits.

Click here to learn more about five ways companies using digital manufacturing are greening their supply chains.

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Company News

AREVA Names ANSYS Certified Supplier

21 July 2009

ANSYS, Inc. has been awarded an AREVA Certified Supplier seal of approval, strengthening the relationship between the two organizations. As a world leader in the nuclear power industry, AREVA works with key suppliers in its efforts to expand operations and develop new markets. It named ANSYS among 170 U.S. and Canadian companies that received this mark of distinction, citing how essential AREVA's partners are in deploying activities that support the company's growth.

Becoming an AREVA Certified Supplier entailed meeting 25 criteria, such as quality, sustainable development values and competitiveness. Other decisive areas included investment in innovation and R&D, capacity to tackle new markets, and attention to nuclear/occupational safety and the environment.

"With this distinction, AREVA announces that it intends more than ever to strengthen its relationship with the companies that work closely with them," said Jim Cashman, president and CEO of ANSYS, Inc. "AREVA has had a long-standing relationship with ANSYS and has used our products throughout the world in its nuclear energy applications. In fact, ANSYS® is AREVA's standard solution for mechanical analysis across the enterprise. One application example is design optimization for the European Pressurized Reactor (EPR), one of the first GenIII+ reactors under construction. The completed projects deliver a steady stream of energy with increased reactor safeguards."

About AREVA Inc.

In 2008, AREVA purchased nearly $1.5 billion in goods and services from North American suppliers. Together with investments in major infrastructure projects, these purchases are helping AREVA develop CO2-free energy products and services.

As the leading U.S. nuclear vendor and a key player in the electricity transmission and distribution sector, AREVA Inc.'s 6,000 U.S. energy employees are committed to serving the nation and paving the way for the future of the electricity market. With 45 locations across the nation and nearly $2 billion in energy revenues in 2008, AREVA Inc., through its subsidiaries, combines U.S. leadership, access to

worldwide expertise and a proven track record of performance.

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ASCENT Center for Technical Knowledge Releases Three Updated Training Guides for Autodesk ® Software

23 July 2009

RAND Worldwide announced that its courseware division, ASCENT– Center for Technical Knowledge ®, released updated Autodesk ® Training Guides:

• Autodesk ® 3ds Max ® Design 2010 Fundamentals

• AutoCAD ® Architecture 2010 Fundamentals

• Autodesk ® Inventor ® 2010 Advanced Assembly Modeling

ASCENT's Autodesk 3ds Max Design 2010 Fundamentals training guide provides a thorough introduction to Autodesk 3ds Max Design that will help new users make the most of this sophisticated design application, as well as broaden the horizons of existing, self-taught users. With the release of 2010 the new Graphite Modeling ribbon has been incorporated into the training guide.

AutoCAD Architecture 2010 Fundamentals focuses on the design development and construction documentation features of AutoCAD Architecture—the basic tools that the majority of students need in their work. The objective of the training guide is to enable students to work from first concept (conceptual design or mass model) all the way through to design development using the new interface and ribbon features of AutoCAD Architecture 2010.

Building on the skills acquired in the Inventor Introduction to Solid Modeling and Inventor Advanced Part Modeling, Inventor 2010 Advanced Assembly Modeling is designed to take students to a higher level of productivity. The training guide concentrates on the TopDown Design approach for assembly creation and other advanced assembly features aimed at increasing design efficiency. Specifically, this updated training guide teaches the new MultiBody and Layout

Design functionality used for TopDown Design.

"Our expert team of courseware developers is dedicated to assisting our clients in fully leveraging their application's capabilities," said Joe Oswald, Executive VicePresident PLM Operations, RAND Worldwide. "With the release of Inventor 2010 Advanced Assembly Modeling, we have identified the importance of the new TopDown Design workflow and have incorporated the new tools to help users realize the efficiency to be gained with this functionality."

ASCENT is an Authorized Author, Publisher, and Developer of Autodesk ® curriculum. All of the courses authored by ASCENT for Autodesk software are available to educational institutions, individuals, and corporations.

ASCENT will also be releasing Revit Architecture 2010 Intermediate later this month. To see the company's complete courseware lineup for Autodesk, Dassault Systèmes, and PTC software solutions, please visit http://www.ASCENTed.com.

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Autodesk Debuts Clean Tech Partner Program

21 July 2009

At today's Clean Tech Open (CTO) Renewable Energy Symposium, Autodesk introduced the Autodesk Clean Tech Partner Program. The program awards "seed" grants consisting of free bundles of Autodesk software to early-stage, clean technology companies working to solve some of the world's most pressing environmental challenges.

"We understand the significant role design plays in creating a sustainable future," said Lynelle Cameron, director of sustainability for Autodesk. "The Autodesk Clean Tech Partner Program is designed to accelerate innovation and leadership in the clean tech market. As part of our ongoing commitment to global sustainability, Autodesk will be working together with emerging clean tech companies to help bring their ideas to market faster and more cost-effectively."

Recipients of the Autodesk Clean Tech software grant will receive a collection of Autodesk's top applications:

-- Autodesk Inventor Professional

-- Autodesk Showcase Professional

-- Autodesk Vault Manufacturing

-- Autodesk Navisworks Manage

-- Autodesk Revit Architecture

-- Autodesk Alias Design

Each grant has a retail value of up to U.S. $150,000, and will include up to five full commercial licenses of each application.

"Autodesk and the Clean Tech Open are committed to enabling green entrepreneurs expand upon their innovative ideas," said Michael Santullo, co-founder of the CTO. "Many participants in the Clean Tech Open are first-time entrepreneurs - they have a great idea, but could really use some assistance. This is where Clean Tech Open steps in: we connect entrepreneurs with the expertise, talent and funding necessary to create successful, sustainable businesses."

As a precursor to the Clean Tech Partner Program, 13 startups have already received similar packages from Autodesk. Syncromatics was rewarded for its use of sustainable green technology in providing customized solutions for transit agencies nationwide. Autodesk also named the company Inventor of the Month in June. "Autodesk provided critical design and engineering tools that enable our company to rapidly develop quality products. These tools are the cornerstone of our success and have fueled our company's growth and profitability," said Stephen Salazar, chief operating officer of Syncromatics.

Serious Materials, a company that develops and manufactures advanced green building materials designed to save energy and money, also benefitted from an Autodesk seed grant. "Autodesk products allow us to digitally model our prototypes before they're built," said Kevin Surace, Serious Materials chief executive officer. "This has shortened our development and manufacturing cycles and allowed us to bring our products to market much faster."

As a Gold Sponsor of the Clean Tech Open, Autodesk has already teamed with the CTO to help numerous entrepreneurs launch companies. The collaboration is an innovation catalyst, helping great ideas become viable clean tech businesses. In partnering with these emerging clean tech companies,

Autodesk aims to help them make smarter business decisions, save money and collaborate more effectively.

Autodesk has set a goal of awarding clean tech software grants to 100 companies by the end of January 2010. Full program information, including application process details for the Clean Tech software grant, is available at www.autodesk.com/cleantech.

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CADD Centers of Florida Inks SITEOPS® Reseller Agreement with BLUERIDGE Analytics®

23 July 2009

BLUERIDGE Analytics, providers of SITEOPS land development optimization software (http://www.siteops.com), announced that CADD Centers of Florida has signed on as its fourth authorized U.S. reseller.

SITEOPS Design SP, a web-based software tool for preliminary site design, is the initial BLUERIDGE CAD product available via resellers. This design product uses the auto-draw tools from SITEOPS Single Pad and Multi Pad optimization software to enable rapid site selection assessments. Users can create and revise numerous conceptual site layouts, determining whether a building and parking are feasible on single pad sites, with multiple pad capability slated for October.

Gregory Arkin, CADD Centers Vice President, stated, "As we make the transition from 2D to 3D, 4D, and 5D in the AEC industry, SITEOPS is not only an amazing tool, but clearly provides an immense advantage to our customers with its ability to design, calculate and analyze construction and layout feasibility very early in the design process."

Arkin added, "As the largest civil and government reseller in Florida, we are honored to have been selected to partner with SITEOPS to revolutionize the workflow and process for our customers. Whether it's developers, architects, civil engineers or contractors, SITEOPS fits in perfectly with our BIM platform of products. We're very excited about integrating the technology into the AEC industry."

BLUERIDGE kicked off its CAD market reseller program in April 2009, and within three months added five U.S.-based resellers and a referral arrangement in Brazil. Resellers are strategically selected to develop coverage of the U.S. architecture-engineering-construction (AEC) software market, typically without direct competition. This offers resellers a chance to differentiate themselves with a unique SaaS product.

"The response to this program is outstanding," said Al Wojcik, BLUERIDGE Vice President of Sales. "CAD resellers want innovative products that will help their clients produce faster, better designs. Resellers love the SaaS/cloud computing model. Online software means they don't have to stock or ship our products - they can be delivered on-demand."

Land developers, retailers, and civil engineers use SITEOPS Single Pad and Multi Pad to produce site layout options and cost reports to identify substantial savings for commercial and retail properties.

Other SITEOPS Design SP resellers include Holman's of Nevada, U.S. CAD, and Duncan-Parnell.

SITEOPS is "CAD with a Brain" - web-based software that reduces the time and cost of land development. Real estate developers, retailers, and civil engineers use SITEOPS products to perform real-time feasibility simulations and optimize site designs.

Clients include Lowe's Companies, Target, Regency Centers, McIntosh & Associates, and Hendrick Automotive Group, and other leading retailers, civil engineers, architects, and land developers.

Charlotte-based BLUERIDGE Analytics delivers computing software to target markets in retail, real estate, and AEC industries.

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Mastercam Announces 4th Annual "Innovator of the Future"; Contest winner designs exceptional motorcycle gas cap

July 2009

CNC Software has announced the winner of its 2008-2009 IOF (Innovator of the Future) competition: Justin Amos, a student in the Advanced Manufacturing Program at Vincennes University (Vincennes, Indiana).

Mastercam's Innovator of the Future competition helps introduce students to real-world manufacturing by challenging them to put their own creative twist on a specific part to be judged by a special guest from the manufacturing industry. In the 2008-2009 competition, students created one-of-a-kind motorcycle gas caps for guest judge Jim Quinn of Orange County Choppers. Prizes were a major motivation for students with the winner receiving a $1,000 scholarship and a trip to Newburgh, New York to tour the Orange County Choppers world headquarters.

In the documentation accompanying their entries, the students each explained how the competition helped them to improve their Mastercam and machining skills. With many excellent entries, competition was fierce. Justin Amos was chosen as the winner, with a cap featuring an F-16 soaring over a compass design with a spinning brass arrow. As a pilot, Justin has always enjoyed the jet-themed bikes made by the OCC team.

When asked his opinion about the IOF competition, Justin enthusiastically replied, "It's a great contest!"

As a student who often struggled to find motivation in school, Justin found that the IOF competition inspired him to go above and beyond. He enjoyed that the competition provided certain parameters but also gave him a lot of room for creativity. This freedom to design a part that appealed to him is what motivated him and excited him about school.

While the $1,000 scholarship will undoubtedly help to defray educational expenses, Justin really enjoyed his trip to tour the Orange County Choppers shop. Lead Engineer, Jim Quinn, took a few hours out of his busy schedule and gave him an in-depth behind-the-scenes tour focusing on the machine shop complete with numerous anecdotes about projects and builds. Best of all was the opportunity to spend some time with Jim Quinn. Justin hopes to one day work in a custom hot rod shop and was very interested to hear about what Jim's day-to-day life at OCC is like.

In addition to choosing the winner of the competition, Jim Quinn named two runners up. With a vintage-style cap featuring both brass and aluminum, Brian Flenar from Vincennes University was named the first runner-up. Second runner-up, Gregg Nemec from Dunwoody College of Technology (Minneapolis, Minnesota), created a cap that featured an old school OCC-style dagger.

For more information on Orange County Choppers, go to http://www.orangecountychoppers.com. For more information on the Mastercam Innovator of the Future competition please visit http://www.mastercam.com/IOF

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MSC.Software Creates Customer Advisory Board

23 July 2009

MSC.Software Corp. announced the creation of a Customer Advisory Board (CAB) that will align MSC.Software products and business practices with recognized thought leaders in automotive, aerospace, energy, manufacturing and other industries. The shared objectives of the CAB members are to identify and accelerate the availability of critical technologies within commercial Computer Aided Engineering (CAE) tools, align technology priorities within and across industries, and help establish business policies and procedures that make it easier for customers to work with MSC.

Eighteen industry leaders have agreed to become initial members of the CAB including VIF (Virtual Vehicle Competence Center), SIKORSKY, The Boeing Company, GOODRICH, Airbus, Tata Motors, Lloyd's Register, Mitsubishi Motors, EADS, and GKN. Members will meet on a quarterly basis with MSC.Software senior management to discuss, debate, and have open dialogue on industry trends, business & technology drivers, key customer issues, and market opportunities. This interaction will provide MSC and the CAB members with critical insight into details of the issues that are facing product development organizations today, including CAE technology and how that technology is delivered to industry.

"Participation in MSC.Software's Customer Advisory Board will make our existing strategic relationship even more valuable. Accelerated delivery of critical technologies aligned to our needs will result in competitive advantage to GKN and the other CAB members", said Steve Minter, Vice President of Engineering at GKN Driveline.

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Omnify Software Helps Medical Device Customers Automate Training Processes

20 July 2009

Omnify Software announced that medical device customers are leveraging the Omnify Empower PLM solution to automate product development and training processes for Food and Drug Administration (FDA) and International Standards Organization (ISO) compliance.

In addition to providing a single location to track and manage all product data through an automated process, a key benefit of Omnify Empower PLM for medical device manufacturers is Omnify's training management functionality. Companies that need to meet FDA and/or ISO regulations are required to implement and document employee training. Incorporating Training Management within the Omnify system not only eliminates the need for customers to purchase and manage a separate training solution, it associates training events with all product and project data stored in the Omnify database.

Procedures and product training are constantly changing, particularly with medical devices. With Omnify, customers are able to have training as part of the engineering change process to track product and procedure revisions, automatically configure new training requirements and generate new training alerts for affected personnel. This ensures all appropriate parties are notified and guarantees training requirements are fulfilled.

PLC Medical Systems, Inc., a company focused on innovative cardiac and vascular medical device-

based technologies, is one of many customers meeting compliance by leveraging Omnify Empower PLM to manage product development and training processes. "In our most recent ISO compliance audit, Omnify Empower was noted as a significant enhancement and a demonstration of our commitment to continuous improvement," stated Jeff Steward, director of IT for PLC Medical Systems, Inc. "Having our training process automated and managed in Omnify helps to determine if people were actually trained and lets us know who was notified, when and on what, which is very important for us or anyone looking to be FDA or ISO compliant."

"Omnify Empower PLM provides medical device manufacturers with a solution that delivers the functionality to support their product development and compliance needs in one central location," stated Chuck Cimalore, CTO for Omnify Software. "Incorporating features such as a closed-loop Corrective and Preventive Action system and training records management into the PLM suite is the result of working closely with customers like PLC Medical Systems in order to provide a system that truly delivers complete product record management."

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OVM World Collaborates on Accellera's Industry Solution for VIP Interoperability

22 July 2009

Mentor Graphics and Cadence Design Systems, Inc. announced that the Accellera guide for verification IP (VIP) interoperability, currently in draft form, was enabled by technology contributions provided by both companies in open source form, and served as a basis for the reference implementation of the Accellera VIP Technical Sub-Committee (TSC) "Best Practices" guide. The guide provides recommendations for interoperability between verification components compliant with the Open Verification Methodology (OVM) and those developed using legacy methodologies such as the approach documented in the Verification Methodology Manual (VMM).

Historically, advanced verification users have had to invest a great deal of time and effort to develop verification environments with VIP from different sources. At the same time that the Accellera VIP TSC was framing the requirements for an interoperability solution, Cadence® and Mentor, working with leading customers, members of the OVM Advisory Group (OAG), and other industry participants, developed a set of library components fulfilling these requirements. This reference implementation was a key to validating the draft Accellera interoperability guide, which incorporates many portions of the documentation developed by Mentor, Cadence, and their OVM World partners.

"Our customers embraced the OVM very quickly when it was introduced two years ago, but communicated clearly that they wanted to include legacy VIP without having to re-write it from scratch," said Dennis Brophy, director of strategic business development at Mentor Graphics. "We took a lead role in Accellera to define the industry requirements while working with our OVM partners to develop an interoperability solution. We are pleased to see the results of our efforts reflected in the draft guide that Accellera is in the process of making a standard."

All aspects of the reference implementation are compliant with IEEE Std. 1800-2005 SystemVerilog and have been thoroughly verified using OVM 2.0.1 on the Cadence Incisive® and Mentor Questa verification solutions. The VIP interoperability approach documented in the draft Accellera guide enables users to integrate VIP written in standard IEEE verification and modeling languages and legacy methodologies. This minimizes the need to re-write existing VIP when setting up an OVM-based verification environment, a clear savings in cost and time to market for users.

"With our long history of support for SystemC models and e-based verification, our customers required a solution that spanned these two languages as well as SystemVerilog," said Stan Krolikoski, group director, standards and ecosystem at Cadence. "Our leadership in the Accellera VIP TSC ensured that the scope of interoperability would span multiple languages and multiple methodologies. The OVM is robust enough to provide a complete solution for all of our customers, so we strongly support the draft Accellera interoperability guide and its recommended best practices."

About the Open Verification Methodology

The Open Verification Methodology is the first open, language-interoperable, verification methodology in the industry. It provides a methodology and accompanying libraries that allow users to create modular, reusable verification environments in which components communicate with each other via standard transaction-level modeling interfaces. It also enables intra- and inter-company reuse through a common methodology and classes for virtual sequences and block-to-system reuse, and full integration with other languages commonly used in production flows. The OVM and OVM World began in August 2007 as a joint effort by Cadence Design Systems and Mentor Graphics.

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Tata Technologies Launches i SUPPORT IT™ – Four-tiered Solution for PLM and Engineering Professionals

20 July 2009

Tata Technologies announced the launch of i SUPPORT IT, its proprietary four-tiered solution that fuses essential and comprehensive support services for PLM and engineering professionals.

i SUPPORT IT provides scalable support solutions to clients, that range from no-cost, self-help through enterprise-level agreements. This is possible through the integration of Web-enabled support, live support, and i GET IT® online knowledge management capabilities delivered through these four packages:

1. i SUPPORT IT Web Help – Web-enabled support that includes 24/7 online access and access to the i GET IT online community.

2. i SUPPORT IT Live Help – All the Web-based support, with the addition of entry-level phone support and single-action HelpDesk support.

3. i SUPPORT IT Multi-Application – Adds multi-application HelpDesk support

4. i SUPPORT IT Enterprise – Fully covers the extended organization

"Every Tata Technologies client receives a free i SUPPORT IT Web Help account, providing them access to more than 100,000 knowledge documents, and including access to all the community features on i GET IT," said David Fedler, Tata Technologies Chief Knowledge Officer. "With more than 115,000 users in 60 countries currently relying on i GET IT for Web self-help, these options that are available to expand their support solutions are designed to enhance their investment in PLM technology.

"Productivity and profitability are the ultimate goals of every organization, and timely and accurate support for systems and applications is critical to those pursuits," he added.

i SUPPORT IT has already proven its value to clients, as these testimonials from client evaluations demonstrate:

• “The i SUPPORT IT staff (is) always very helpful and understands that not everyone is at the same level (of) software understanding … they take the time to make sure you have full control of the issue before leaving you ... Very satisfied.”

• “Simply said, it was the best decision I've ever made to purchase products and services form you folks. Your (technical team) is a tremendous asset to us. Once again, I couldn't be happier!”

• The i SUPPORT IT team did all they could to help me. They even called my software OEM for help on the issue and remained (involved) until they were sure that the OEM understood, and could solve, the problem. Special thanks to all of the support people. I spoke to several and each one was able to pickup and help, or direct me to the person who worked with me previously.”

To learn more about i SUPPORT IT, visit http://www.myisupportit.com or e-mail to isupportit@tatatechnologies.com.

About i GET IT®

i GET IT is a comprehensive online knowledge management tool designed specifically for engineers. With more than 100,000 subscribers, in more than 60 countries, i GET IT offers more than 100,000 hours of professional online training, engineering tech tips, forums, blogs, practical online tools, leader board recognition, engineering industry news, and other relevant information for engineers. http://www.myigetit.com

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Events News

Apache Design Solutions to Host Customer Presentations and Hands-On Tutorials at Design Automation Conference

21 July 2009

In booth #722 at the 46th Design Automation Conference (DAC) in San Francisco CA, Apache Design Solutions will host presentations by leading semiconductor companies on their methodologies for addressing power and noise challenges and their experiences with Apache’s tools. The company will demonstrate recently announced Totem power, noise, and reliability platform for analog, mixed-signal, memory, and high-speed I/O designs, as well as RedHawk-NX, a next generation SoC power integrity solution and Sentinel, a chip-package-system co-analysis and co-optimization solution for IC package, board, and SiP designs. In addition, hands-on tutorial sessions will be conducted to provide first-hand experience with Totem and RedHawk. For presentation details and registration, go to http://www.apache-da.com/apache-da/Home/NewsandEvents/Seminars.html.

What: Customer presentations; product and technology roadmap presentations; hands-on tutorial sessions

Where: Apache Design Solutions, Booth #722, South Hall

Design Automation Conference, Moscone Convention Center, San Francisco CA

When: Rambus: High-speed I/O interface supply noise and reliability analysis

Monday, July 27, 1:00 p.m.

TSMC: SiP opportunities and design challenges

Tuesday, July 28, 11:00 a.m.

Broadcom: Prototyping to sign-off of 45nm Broadcom Mobility Chip design

Tuesday, July 28, 1:00 p.m.

Totem Hands-on Tutorial

Monday, July 27, 3:00 p.m.

RedHawk Hands-on Tutorial

Tuesday, July 28, 3:00 p.m.

RedHawk, Totem, and Sentinel presentation and demonstration

July 27 – July 29, 10:00 a.m. – 6:00 p.m.

July 30, 10:00 a.m. – 1:00 p.m.

Additional Presentations at DAC by Apache Design Solutions:

In the Exhibitor Forum (booth #4359), Apache Design Solutions will be presenting "De-Risking Your Design from Power Noise Impact" on July 27 at 2:00 p.m. and "Power and Substrate Noise Analysis and Design Optimization for High-performance Analog and Custom Design" on July 29 at 1:00 p.m.

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CGTech to Show VERICUT 7 at Offshore Europe 2009

24 July 2009

CGTech will exhibit the next major version of VERICUT CNC machine simulation and optimisation software on Stand 1138 at Offshore Europe, Aberdeen, September 8th – 11th.

VERICUT is software that provides a virtual machine tool environment where CNC programmers can test and optimize CNC programs without using any valuable time on a real CNC machine. This is particularly useful with complex multi-axis, multi-function CNC machines which are used extensively in the Oil and Gas industries.

The stand at OE2009 will feature a simulation gallery showing examples of VERICUT applications in the Oil and Gas, Power Generation, Aerospace and Automotive industries. Simulations will be included for all the leading CNC Machine Tool manufacturers including DMG, Mori Seiki, Makino, Matsuura, Mazak, WFL, Hermle and Chiron.

VERICUT is used by the world's leading manufacturing companies and features interfaces to all the leading CAD/CAM/PLM systems including Catia V5, Siemens NX, PTC, MasterCAM, EdgeCAM and

GibbsCAM, and interfaces are also available from Delcam, for PowerMill, Open Mind for HyperMill, and Missler for TopSolidCAM.

VERICUT 7 features significant performance-improving enhancements that reduce the time required for manufacturing engineers to develop, analyze, inspect and document the CNC programming and machining process. Instead of focusing on new features or add-on modules, CGTech developer resources have focused on diligent code optimization and customer-driven enhancements.

“VERICUT has been reorganized with a new user interface for maximum efficiency” Said Bill Hasenjaeger, Product Marketing Manager. “Not only is the software extremely stable and significantly faster, it has never been easier to set up a VERICUT project. This release will set a new standard for the world’s most advanced CNC simulation system.”

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COADE Announces Drivers of Success Competition Entry Deadline of July 31, in Conjunction with COADE User Conference

23 July 2009

COADE announced a 2009 Drivers of Success Competition entry deadline of July 31, 2009, a competition for users of COADE plant design and engineering analysis products, including CAESAR II, CADWorx, PV Elite and TANK, where users can receive valuable prizes for the best stories about successes using these products. The 10 first-place prize winners receive an all-inclusive trip to this year's 2009 COADE User Conference, and the 10 runner-up prize winners receive an Apple iPod Nano. There will be three first-place and three runner-up prizes for CAESAR II submissions, three first-place and three runner-up prizes for CADWorx, three first-place and three runner-up prizes for PV Elite (and PV Fabricator), and one first-place and one runner-up prize for TANK. Every user submitting a story will receive a valuable token from COADE in appreciation for taking the time to prepare a submission.

Recently, the company also announced an extension the early-bird discount until August 1, 2009, to register for the COADE User Conference, scheduled for September 28-30 in Houston, Texas. The 2009 COADE User Conference will feature product-specific sessions on all of COADE's products, including CAESAR II, its pipe stress analysis software; PVElite for pressure vessel and heat exchanger design and analysis; the CADWorx Plant Design Suite for intelligent plant design modeling and process schematics; and TANK for the design and analysis of oil storage tanks. A keynote address will be delivered by Thomas J Van Laan, PE, President and CEO of COADE.

Details on the 2009 COADE User Conference are at http://www.coadeuserconference.com/2009/. Read one of last year's Drivers of Success winner's stories at http://coade.typepad.com/coadeinsider/2009/01/success-story-stantec.html. Details on the Drivers of Success Competition can be found at http://www.coadeuserconference.com/2009/competition.html.

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Design Automation Conference Professional Development Fund to Award More Than $80,000 This Year

24 July 2009

The Design Automation Conference (DAC) announced that for the 16th year, DAC, along with its

sponsors, is awarding more than $80,000 in development funds to students and professionals in the EDA field. More than $2.3 million have been awarded since the inception of the Professional Development Fund. The 46th DAC will be held July 26 – 31 at the Moscone Center in San Francisco.

The DAC Professional Development Fund supports a range of programs, including the A. Richard Newton Graduate Scholarships; the P.O. Pistilli Advancement in Computer Science and Electrical Engineering Program; the Young Student Support Program; the University Booth Program; and several workshops that take place during DAC, such as the Workshop for Women in Design Automation (WWINDA) and the Design Automation Summer School (DASS). The fund also supports the Alumni Scholarship program, which offers DAC alumni who are between jobs an opportunity to attend DAC for professional skills maintenance and development.

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46th Design Automation Conference Welcomes 29 New Exhibitors

20 July 2009

The Design Automation Conference (DAC) announced that it will feature 29 companies exhibiting at this year's conference for the first time. The new exhibitors include companies ranging from providers of design tools and data management solutions to product development experts and placement firms. The 46th DAC will be held July 26 – 31 at the Moscone Center in San Francisco and DAC exhibit hours will be 9 a.m. to 6 p.m. Monday, July 27 through Wednesday, July 29 and 9 a.m. to 1 p.m. on Thursday, July 30.

This year, the DAC exhibit floor features almost 200 companies. Access to exhibits is available through full-conference, exhibit-only, or Free Monday registration. Exhibit-only registration offers access to all four days of the Exhibition, the keynote sessions, including the plenary CEO keynote panel, all DAC Pavilion and Exhibitor Forum sessions, plus the new IC Design Central Partner pavilion. Free Monday registration permits access to the exhibition and the plenary CEO keynote panel on Monday, July 27.

"This robust list of first-time DAC exhibitors reflects the diversity of the innovation taking place in the industry, and reflects the role DAC plays as the premier venue for introducing new solutions and connecting with customers and partners," said Andrew B. Kahng, general chair, 46th DAC Executive Committee. "We are very pleased to welcome this year's new exhibitors, and we look forward to the excitement they will bring to the exhibit floor."

The following companies and organizations will be exhibiting at DAC for the first time this year:

Achilles Test Systems Inc.

Agnisys Inc.

Altair Engineering Inc.

AnSyn

APAC IC Layout Consultant Inc.

ATEEDA Limited

BEEcube

Cambridge Analog Technologies Inc.

Chipworks

CST of America Inc.

Desaut Inc.

DOCEA Power

E-System Design Inc.

Enterpoint

Epoch Microelectronics Inc.

Fidus Systems Inc.

Innovative Logic Inc.

Logic Perspective Technology Inc.

Mephisto Design Automation

MethodICs LLC

NextOp Software Inc.

Optiwave Systems Inc.

OVM World

R^3 Logic Inc.

SKILLCAD INC.

Tiempo

Warthman Associates

XJTAG

Z^2 Innovation

Registration

For more details on DAC and to register, please visit www.dac.com.

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Free Monday at DAC Includes Six Pavilion Programs

21 July 2009

The Electronic Design Automation Consortium (EDAC) is sponsoring the Free Monday exhibit program on Monday, July 27 at the 46th Design Automation Conference (DAC). In addition to the exhibition, Exhibitor Forum, IC Design Central Pavilion, and the Keynote Panel, Free Monday registration includes

access to the DAC Pavilion (Booth #1928) where six Pavilion programs will be presented that day. DAC will take place July 26 – 31, 2009 at the Moscone Center in San Francisco.

"Everyone in the EDA industry should be at DAC on Free Monday and they will not want to miss the presentations in the Pavilion," said Greg Spirakis, chair of the panels committee for the 46th DAC. "From Gary's Smith's annual 'What's Hot at DAC' session in the morning, to discussions of system level sign-off and protecting IP, these sessions on Monday are sure to be very popular."

The full schedule for the DAC Pavilion on Monday, July 27 is:

9:30 to 10:30 a.m. – Gary Smith on EDA: Trends and What's Hot at DAC

10:45 to 11:45 a.m. – The EDA Heritage Series: Doug Fairbairn's Industry Retrospective

1 to 2 p.m. – Hogan's Heroes: The Long Road to System-Level Sign-Off

2:30 to 3:15 p.m. – IP at Risk: Protecting the Company Jewels

3:30 to 4:30 p.m. – A Conversation with the 2009 Marie R. Pistilli Award Winner

5 to 6 p.m. – DAC/ISSCC Student Design Contest Awards Presentation

The DAC Pavilion Panel program runs through Thursday, July 30 and includes 20 informative sessions that encourage audience interaction. To see the complete list of pavilion panels, visit http://www.dac.com/events/searchevents.aspx?EventType=Pavilion%20Panel&confid=95**.**

Registration

For more information, and to register for either Free Monday, Exhibits-Only or Full Conference attendance at DAC visit www.dac.com or go directly to https://reg.mpassociates.com/reglive/register.aspx?confid=95. All DAC registration, including Free Monday, will also be available onsite.

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Meet at DAC with Leading IP Suppliers During ChipEstimate.com's IP Talks!

22 July 2009

What

IP Talks! returns to DAC for its third year, providing an opportunity for conference attendees to meet with leading IP suppliers to learn how the latest in semiconductor IP can help them accelerate their design success. Supported by the ChipEstimate.com chip planning ecosystem, IP Talks! features 20 ChipEstimate.com partners delivering technical presentations on the latest in semiconductor IP.

When

IP Talks! will be held July 27-30. To view the entire schedule please visit http://www.chipestimate.com/dac2009/.

Where

IP Talks! will take place at the ChipEstimate.com Booth 1100, in the South Hall of Moscone Center in San Francisco.

About ChipEstimate.com

The ChipEstimate.com chip planning portal is an ecosystem comprised of over 200 of the world's largest IP suppliers and foundries. These companies all share in the common vision of helping the worldwide electronics design community achieve greater profitability and success. To date, a diverse global audience of over 22,000 users has joined the ChipEstimate.com community and has collectively performed over 80,000 chip estimations. ChipEstimate.com is a property of Cadence Design Systems, Inc.

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Si2 Announces Annual Member/Guest Meeting at DAC

22 July 2009

Silicon Integration Initiative (Si2) announced the Annual Si2 Member/Guest Meeting to be held on July 27, 2009, from 6PM-8PM, at the Moscone Convention Center, Room 220, in conjunction with the Design Automation Conference. The Meeting is open to both member and non-member companies and individuals who are interested in Si2 activities such as OpenAccess, DFM, and low-power design. A Happy Hour will be held at the beginning and end of the meeting with refreshments and light hors d'oeuvres.

The keynote speaker will be Keith Barkley, senior engineer, Advanced Processor Design, IBM. His topic will be "OpenAccess Enables IBM's Processor Design Success."

Steve Schulz, President & CEO of Si2, and Sumit DasGupta, senior vice president of engineering, will present an outline of Si2's activities and accomplishments of the past year and directions for the year ahead, and will also announce the newly-elected members of Si2's Board of Directors.

To register for this event, leave a message at this link: http://www.si2.org/?page=3.

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STMicroelectronics Unveils Latest Advances in Design Methodologies at DAC 2009

24 July 2009

STMicroelectronics will participate as presenter or co-author of several papers at the DAC 2009 (Design Automation Conference), which takes place from July 26-31, 2009, in San Francisco, California. ST's contributions to the conference cover advances in design methodologies and automation in the areas of 3-D stacking for complex SoC (System-on-Chip) ICs, physical- and system-level chip design, and IC reliability.

In the DAC 2009 'Management Day' session, Philippe Magarshack, STMicroelectronics' General Manager of Central CAD & Design Solutions will present: '3-D Stacking: Opportunities and Trends for Consumer SoCs', which will discuss 3-D integration as a promising technology to extend the momentum of Moore's Law into the next decade, offering higher transistor density, faster interconnects, heterogeneous technology integration, with potentially lower power, cost and faster time-to-market. However, 3-D integration isn't without challenges: the presentation discusses the need for a range of new capabilities including process technology, architectures, design methods and tools, and manufacturing-worthy test solutions to be developed before 3-D chips can be mass produced for consumer applications.

Also, as part of the Management Day, Magarshack will participate on the panel 'Making Critical

Decisions for Emerging SoC Development,' which will discuss emerging solutions for complex nanometer SoCs and their economic impact.

ST is also presenting several papers in physical and system-level design, including the examination of architectural-level design and power-estimation techniques, and the design-automation of IP re-use.

The need to design differentiated SoC product derivatives in extremely narrow time windows is tackled by a paper from ST engineers. The paper describes the moving of design creation to higher levels of abstraction, presenting an ESL (Electronic System Level) design methodology as a solution to deal with the increasing design challenges in the industry. In addition, the paper explores solutions for optimal designs in terms of power performance and silicon die area.

Another paper describes how ST engineers have used the SPIRIT (Structure for Packaging, Integrating and Re-using IP within Tool flows) Consortium's IP-XACT standards to enable IP reuse through design automation, to provide an SoC integration solution for ST's program (with Freescale) for the fast development of new 32-bit automotive microcontroller families.

An approach to improving design productivity for digital consumer ICs is the subject of another paper. ST's engineers propose allowing front-end designers to prototype the SoC at the architecture level, gaining early insight into potential implementation issues during the design capture stage.

Power management, also, is an increasingly important concern for both wireless and wired applications. ST engineers will present an architectural-level power planning and estimation system to manage the challenges to preserve power and extend battery life in portable products.

Testing and reliability are also addressed by ST's engineers, in two papers. The first paper is a presentation on a low-power DFT (Design-For-Test) flow for multi-voltage designs and ATPG (Automatic Test Pattern Generation). The second paper examines an approach for the reduction of EMI (Electromagnetic Interference) to produce very robust automotive IC designs.

Further information about DAC 2009 and ST's papers is available at:
http://www.dac.com/46th/index.aspx

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Unleashing High-Performance Compute Clouds to Overcome EDA Challenges; PBS GridWorks CTO at DAC conference to address management of time-critical EDA workloads by leveraging cloud computing

24 July 2009

Altair Engineering, Inc. announced that Dr. Bill Nitzberg, the chief technology officer for its on-demand computing division, PBS GridWorks, will discuss cloud computing as a viable solution to cost-effectively manage complex EDA compute workloads during the upcoming Design Automation Conference in San Francisco on Wednesday, July 29, beginning at 2:30 p.m.

"Cost-effective cloud computing requires powerful tools that can match constantly changing workloads with available resources to more efficiently use all resources," said Dr. Nitzberg. "The benefits allow companies and organizations of all sizes to maximize the utilization of HPC resources, make data-driven IT planning and purchasing decisions, manage complex application workloads and minimize the energy consumed by computing assets."

The 46th Design Automation Conference (DAC) convenes in San Francisco, California. DAC features a

wide array of technical presentations, plus more than 200 of the leading electronics design suppliers. For more information and to register, visit http://www.dac.com.

Dr. Bill Nitzberg and PBS GridWorks technical representatives will be on hand throughout the DAC conference (Booth 4208) to answer questions and to provide an overview of the new release of PBS GridWorks.

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Financial News

IFS Interim Report, January–June 2009

17 July 2009

January-June 2009

IFS reports improved EBIT and strongest cash flow to date

Net revenue amounted to SKr 640 million (606) during the second quarter, a growth of 6% including, and a decrease of 3% excluding, exchange rate differences.

Product revenue increased by 1% to SKr 279 million (276) during the second quarter: license revenue decreased by SKr 25 million to SKr 86 million (111) whereas maintenance and support revenue increased by SKr 28 million to SKr 193 million (165).

Consulting revenue increased by 10% to SKr 357 million (324) during the second quarter.

EBIT for the second quarter amounted to SKr 33 million (4).

Cash flow after investments during the second quarter amounted to SKr 32 million (–46).

Cash flow after investments for 12 months rolling amounted to SKr 163 million (151).

Net revenue increased to SKr 1,274 million (1,162) during the first six months.

Earnings for the first six months amounted to SKr 27 million (1), with earnings per share after dilution amounting to SKr 1.00 (0.04).

Interim Report 2009 Q2 — PDF-file (223 KB)

Interim Report 2009 Q2 Presentation — PDF-file (475 KB)

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Implementation Investments

Autodesk Helps Bring Automotive Design Data from CAD to Ad

22 July 2009

Autodesk, Inc. announced that the BMW Group has contracted Autodesk Consulting to automate the transformation of design data into marketing assets and create photorealistic, animated models of BMW, MINI and Rolls-Royce brand cars. Autodesk, in cooperation with Mackevision, will convert vehicle data into Autodesk Maya and Autodesk Showcase software files that are ready for animation and rendering.

These photo-real virtual models will be used to create marketing materials before the vehicles are actually produced -- including TV commercials, brochures and the company's web profile.

"Leveraging design data for marketing is revolutionizing how the automotive industry advertises in print, on the web and in television commercials," said Karim Salabi, Autodesk vice president, Visual Communication Group. "Using computer software to generate advertising visualizations allows automotive agencies to market their new vehicles without costly physical prototypes. This approach also unlocks new creative potential, empowering advertisers to create compelling art direction that is difficult and very expensive to do with traditional photography."

Together with Mackevision, Autodesk will create more than 240 virtual models of the BMW Group vehicles over the next three years. Autodesk Consulting will provide Autodesk Creative Bridge services to architect a visual workflow for BMW that leverages their 3D assets to lower production costs, while enhancing creative flexibility. Mackevision -- a company specializing in computer-aided visualization of vehicle data -- will process an extensive design data pipeline under the management of Autodesk's consulting team.

Showcase software, part of the Autodesk solution for Digital Prototyping, helps create accurate, realistic and compelling imagery from 3D CAD data to convey form and create environmental context to communicate brand character. Autodesk Maya is a powerful, integrated 3D modeling, animation, and rendering solution that enables consumer products and automotive manufacturers to incorporate CAD data into engaging product collateral. Maya is a natural extension of the Autodesk Alias family of products and Autodesk Showcase for the creation of advanced rendering and animated visualizations of digital prototypes.

About Mackevision

Mackevision is a premium creative system partner for image communication. As experts in 3D visualization, animation, post production and visual effects, the company designs and produces high-quality images and film footage. Mackevision also develops independent image production solutions for international agencies, film productions and industrial clients in the automotive, architectural, pharmaceutical and consumer product industries. From data preparation through creative design, implementation of projects and production, Mackevision provides all computer-aided processes for 3D visualization and film production.

Mackevision's development department has introduced the F_BOX product family. With the F_BOX product family industrial customers, photographers and agencies can configure high-quality 3D visualizations for marketing and information materials, based on edited product data, easily and economically.

Mackevision Medien Design GmbH was founded in 1994. The company's headquarters is located in Stuttgart, with branch operations in Munich and Detroit. For more information about Mackevision, visit www.mackevision.com.

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Delta Marine Steers Ships in the Right Direction Using ANSYS Engineering Simulation

20 July 2009

ANSYS, Inc. announced that Delta Marine Engineering Co., a merchant marine designer based in Turkey, uses Simulation Driven Product Development™ from ANSYS to optimize ships that transport

cargo to all points of the globe. The company analyzes its designs with software from ANSYS to identify and correct troublesome vibration, in order to comply with international standards as well as ensure the safety of the crew and a long life for the ship.

One of the most basic tasks that marine engineers face is eliminating undesirable vibration. Each ship has natural frequencies dependent on the design of its structure, which includes parameters such as size and shape as well as the materials used. In addition, there are forcing frequencies that act upon a ship, most often generated by components that operate at different frequencies. As the propeller moves the water, for example, it exerts forces on the back of the ship, and these forces are large enough that they can cause vibration, particularly if they excite one of the structure's natural modes of vibration.

An ocean-going capesize bulk carrier, which can carry bulk cargo such as iron ore or coal up to 180,000 tons, is continuously slammed. The propeller alone can exert loads of 10 tons to 14 tons, and the engine can generate additional moments up to 200 tonmeters. Vibration in marine applications is especially complex because it also involves the behavior of the structure as it passes through the water. This fluid structure interaction (FSI) can fatigue the hull's components and cause vital equipment to malfunction.

"Simulation analysis gives our engineers insight into the complexities of these interactions," said Dirim Sener, planning director, Delta Marine Engineering Co. "Using ANSYS® technology, our engineers try to correct problems by modifying the ship during the design stage — instead of discovering vibration problems after the ship is launched." He added that changes made after launch could cost millions of dollars, while changing the underwater form of a ship in the design stage can be done at almost zero cost. "Engineers also have much more freedom when making design changes in the early stages."

Delta Marine engineers use software from ANSYS to calculate pressures induced by the propeller on the aft of the ship as well as the loads generated on the propeller shaft. If vibration values do not meet international standards, sometimes expensive changes must be made. By identifying vibration problems in the early stages of the design process, Delta Marine can make alterations such as adding pillars or strengthening structural components, or changing the propeller, revolutions per minute of the crankshaft, or number of blades in the propeller. Then, engineers can update the model to determine the effect of the changes on vibration displacement and velocity.

"The marine industry is challenged to develop and produce new designs at an accelerating pace. Designing ships is not a straight-forward process: The changes are frequent and prototyping can be quite expensive. Delta Marine has shown how Simulation Driven Product Development can be extremely effective in designing vessels that mitigate risk — helping engineers make critical decisions throughout the design process," said Dipankar Choudhury, vice president, corporate product strategy and planning, ANSYS, Inc.

Delta Marine also uses ANSYS technology to evaluate the structure and cargo tanks of ships against worst-case load scenarios involving forces exerted by the tank's contents against the tank itself. For example, the design and construction of sulfur- and bitumen-carrying tankers is complicated by complexity of the cargo tanks, which could either be built independently or as part of an integrated structure.

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Kayser-Roth Goes Live with Visual PLM.net™

1 July 2009

Kayser-Roth Corporation, one of the most successful Legwear and Intimate Apparel manufacturers in America, is officially live on Visual PLM.net™.

The Kayser-Roth team has rolled up its socks (pun intended) and deployed to all its designers, merchandisers, production team and offshore vendors, the browser based Product Lifecycle Management tool "Visual PLM.net™**.**"

As part of its strategic relationship with Visual 2000, Kayser Roth has implemented the Visual PLM.net™ application to support its international Product Development and long-term growth strategy.

The application is being rolled out across all of the leading Legwear and Intimate brands including No nonsense, Hue and Burlington.

To support its international expansion strategy, Kayser Roth has adopted a centralized Product Development business model and is deploying a single instance of the Visual PLM.net™ System across all of its offices.

As part of this effort, Kayser Roth implemented Merchandise Planning, Project Management and the PDM components to orchestrate the data exchanges between Visual PLM.net™ environment, its legacy systems and other new systems.

Kayser Roth will benefit from immediate value with the Visual PLM.net**™** as a result of better data integrity, more efficient and accurate entry and ease of maintenance around the Product Development process.

About Kayser-Roth

The Kayser-Roth Corporation is a major manufacturer and marketer of Hosiery and Intimates products in the United States. Kayser-Roth is headquartered in Greensboro, North Carolina and operates four plants in North Carolina and Tennessee. The company also has a design studio/showroom in the heart of the fashion district in New York City.

Kayser-Roth sells No nonsense® panties, bras, pantyhose, socks, sleepwear and foot comfort products to major food, drug and mass outlets. The company also produces HUE® socks, Legwear and Intimate Apparel for major department and specialty stores, in addition to producing Calvin Klein hosiery, PrimaSport, Burlington Hosiery and Burlington Socks, and private label programs for major retailers.

Kayser-Roth is an affiliate of Golden Lady, a privately owned Legwear company headquartered in Mantova, Italy.

About Visual PLM.net™

Visual PLM.net™ is a full featured Product Lifecycle Management software solution. A multi Platform browser based client, Visual PLM.netTM, includes PDM, Merchandise Planning, Multi level Project Management, User and Role based Calendars, Automated internal and external Notification System, Field Based Workflow management, Formulas (Validations, Costing), PDM Interface Designer, Search Designer, Data Integration Manager, Dynamic Reporting Tool.

About Visual 2000 International

Visual 2000 International Inc is a leading provider of Software Solutions to the AFA, Apparel, Footwear and Accessories industry. For more information about Visual 2000 International, please visit http://www.visual-2000.com

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KC Samyang Water Systems Selects Siemens PLM Software to Support Growth

21 July 2009

Siemens PLM Software announced that KC Samyang Water Systems selected Solid Edge® software with synchronous technology and Teamcenter® Express software to accelerate its process of innovation and improve its product development quality, while reducing time-to-market.

KC Samyang is the fifth largest water intake equipment provider in the world. The company has developed water technology for the past 40 years, from industrial water processing systems to wastewater processing systems.

KC Samyang Water Systems will use Teamcenter Express to streamline its processes throughout the plant. The company has conducted a series of customized Solid Edge training sessions for its designers and will use the software for all current and future design processes.

"The key requirement for selecting a PLM solution was to improve our product development capability while enhancing innovation as we continue to integrate with our ERP systems," said Kuk Hyun Kim, project manager, KC Samyang Water Systems. "In our evaluation process Siemens PLM Software's technology helped us achieve our goals better than any other solution on the market."

Teamcenter Express is the collaborative product data management (cPDM) component of the Velocity Series™ portfolio. Solid Edge is a core component of the Velocity Series portfolio and combines the speed and flexibility of direct modeling with the precise control of dimension-driven design, providing a fast, flexible design experience that allows customers to accelerate their design process by up to one hundred times.

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Lawson Signs Enterprise Software Contract with Alternative Apparel

20 July 2009

Lawson Software announced that Alternative Apparel, a U.S.-based manufacturer of apparel and accessories, has signed a contract to implement Lawson QuickStep Fashion, including Lawson e-Sales and Lawson Business Intelligence. The Lawson system will help Alternative Apparel meet its growth objectives by helping to consolidate many business processes into a single, integrated system. The contract was signed during Lawson's fourth quarter of fiscal 2009, which ended May 31, 2009.

Alternative Apparel is a lifestyle apparel brand for men, women and babies/toddlers across the U.S. as well as Canada, Italy, Germany, Australia, Japan and the United Kingdom.

The current business software in use at Alternative Apparel could no longer support new value-adding business processes, such as flexible inventory allocation and improved collaboration with customers and suppliers. The company needed more timely and accurate information for improved decision making.

"We needed to find a standard, industry-tailored solution along with people with fashion industry expertise to implement it," said Evan Toporek, president and COO for Alternative Apparel. "We chose Lawson because we felt a great cultural fit between our organizations and have appreciated the Lawson team's dedication. Lawson QuickStep Fashion will help bring support and transparency throughout our supply chain, from product concept to market."

"Lawson QuickStep Fashion combines industry-specific content with built-in business tools based on

Lawson's experience and knowledge of the fashion industry," said Andrew Dalziel, global marketing director for Fashion at Lawson. "With more than 350 fashion customers globally, Lawson can offer businesses industry knowledge and industry-specific functionality that help fashion companies with a complex supply chain and pressured time-to-market achieve their goals."

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Magma Announces Toshiba Corporation Deploys Talus for 90-, 65- and 40-nm ASICs and ASSPs

22 July 2009

Magma Design Automation Inc. announced that Toshiba Corporation, the world's leading supplier of semiconductors for consumer electronics, has deployed Magma's Talus® IC implementation software for developing ICs at 90-, 65- and 40-nanometer (nm) process nodes that target multimedia, networking and printer applications, in Toshiba worldwide design centers. Toshiba adopted Talus after an extensive evaluation that proved the software's ability to reduce turnaround time, increase designer productivity and improve quality of results. Toshiba deployed Magma design implementation software in Toshiba's Apex flows in 2001, and now has finished multiple designs including 65-nm and 40-nm tapeouts using Talus through its Apex 4.0 flow.

"Toshiba has demanding delivery schedules and performance requirements, and Magma has been instrumental in enabling us to address ever-increasing design and market challenges," said Takashi Yoshimori, Assistant Chief Technology Executive of SoC design, Semiconductor Company, Toshiba Corporation. "Talus recently allowed us to reduce turnaround time drastically and improve leakage power and area for a multi-mode SoC design with more than 10 million gates. Based on this achievement and proven track record, we are now implementing our 90-, 65- and 40-nm designs with Talus."

"For Toshiba and its customers, reducing turnaround time is key," said Premal Buch, general manager of Magma's Design Implementation Business Unit. "Toshiba's adoption of Talus firmly establishes Magma's software as the fastest path to silicon."

Talus: The Platform for Nanometer IC Design

Magma's Talus IC implementation is a completely unified RTL-to-GDSII system with advanced capabilities for nanometer design. To address shorter time-to-market windows, Talus is the first implementation solution to multi-process the entire IC design flow. Its front-end design system provides logic designers with a fast, high-capacity, physically aware synthesis capability. Its physical design system addresses variability and multi-mode/multi-corner complexity with new optimization, place and route, and clock tree synthesis technology. To reduce leakage and dynamic power, Talus also provides a complete low-power design system. To improve manufacturability and reliability, Talus provides built-in design-for-manufacturing (DFM) features such as redundant via and litho-aware routing for yield optimization.

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Magma's Talus Enables eSilicon to Implement 400-Million-Gate Designs With 50 Percent Smaller CPU Memory Footprint and 3X Faster Runtime

20 July 2009

Magma® Design Automation Inc., a provider of chip design software, today announced that eSilicon Corporation, a pioneering semiconductor value chain producer (VCP), is completing the implementation of several very large customer designs using the Talus® IC implementation system, including Talus Design, Talus Vortex and Hydra™. These designs are being implemented in a 65-nanometer (nm) process and are more than 500 sq. mm in area, with more than 400 million gates. This is the equivalent of 30 million placeable objects, including more than 100 million bits of memory and more than 2,000 memory instances.

These highly complex chips require eSilicon to use a design solution with extremely high capacity and the ability to deliver fast turnaround on design planning and implementation. In addition, given a tight delivery schedule, eSilicon needed a system that would be usable "out of the box" without a lengthy setup cycle. Magma's field team partnered with the eSilicon design team to deploy Talus.

"We selected Talus for these large designs because of its capacity and our need to minimize our deployment time and keep the implementation cycle as short as possible," said Prasad Subramaniam, vice president of Technology of eSilicon. "The high complexity of these designs poses a significant challenge in productivity and turnaround time. We are pleased that the Talus multi-CPU feature works smoothly and yields significant improvement across a broad implementation flow. We have our default implementation build scripts for large blocks to use two CPUs and we increased to four CPUs for critical runs. This allowed us to gain 1.5 times to 3 times improvement in turnaround time on these large designs."

eSilicon found Talus to be well suited for these designs. Talus' underlying unified data model architecture contains the entire set of data associated with the design. The complete design data can be exported or imported at any time as a Volcano™, Magma's proprietary database format. One of the eSilicon designs is based on a collaborative development model with the customer, and Talus' unified architecture simplifies the efficient handoff of design data via Volcanoes at various points during the implementation process. In addition, Talus' core multi-CPU feature and enhanced GlassBox™ modeling for timing enabled very significant improvement in the turnaround times for implementation and analysis.

One key challenge for these complex chips is the turnaround times for top-level analysis and optimization. eSilicon is making extensive use of a new Hydra GlassBox abstraction capability. This enhanced GlassBox abstraction feature yields extremely compact representations of the blocks that contain all the physical, timing and extraction data necessary for fast and accurate chip-level analysis and optimization without consuming enormous amounts of memory. Because of this new "cached delay" feature for GlassBox abstraction, the latest Talus release requires less than 50 percent of the memory resources required by the previous Talus version and delivers up to a 5X improvement in runtime compared to the previous GlassBox approach.

"The fast deployment of Talus and implementation of these designs is a testament to eSilicon's engineering skill and demonstrates Talus' ability to handle large, complex designs," said Premal Buch, general manager of Magma's Design Implementation Business Unit. "The size of these designs and the speed of deployment demonstrate the major improvements in capacity, runtime and usability that have been engineered into the latest Talus release. It also validates Hydra's capability for managing the top-level design and optimization of very large designs without excessive memory consumption."

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Magnaghi Aeronautica S.p.A. chooses HyperWorks to Streamline Development of Aircraft Landing Gear Systems

23 July 2009

Altair Engineering, Inc. announced that Italy-based aerospace supplier, Magnaghi Aeronautica S.p.A. (http://www.magnaghiaeronautica.it), has chosen the HyperWorks simulation platform to develop and optimize their landing gear systems. The company designs, develops, and manufactures landing gears, hydraulic components, and fuel tanks for the aircraft industry.

"When we first saw HyperWorks and especially HyperMesh during a presentation in Naples last year, we were immediately impressed with its capabilities and flexibility," said Costantino Russo, Chief Deputy within the technical department of Magnaghi Aeronautica S.p.A."We expect remarkable time savings through faster and more automated development processes, and I think that OptiStruct will help us to further reduce both weight and shapes of our components. Particularly, I like the flexibility of the product family, its open architecture and its automated meshing capabilities."

Magnaghi Aeronautica will initially deploy HyperMesh, the suite's finite element pre-processor, and OptiStruct structural optimization technology. Following the initial deployment and training phase, Magnaghi Aeronautica plans to leverage Altair's unit-based software licensing model to explore the suite's twenty-five plus software titles including its finite element solvers and the multi-body dynamics solutions.

"We are very pleased with Magnaghi Aeronautica's decision to chose HyperWorks," said Cosimo Panetta, regional managing director, Altair Engineering Italy. "I see significant time-saving opportunities for the company's entire engineering staff through HyperWorks' advanced morphing capabilities and the ability to automate updates to existing meshes to new design geometries. The adoption of OptiStruct for structural optimization is consistent with a general industry trend that is focused on weight savings – especially in the aerospace industry. We are looking forward to and appreciate the opportunity to work with the engineers of Magnaghi Aeronautica to positively impact their products and business."

About Magnaghi Aeronautica Spa

Magnaghi Aeronautica Spa is part of INVESCO, a leading private Italian aerospace group. Magnaghi was found in 1936 as a company producing landing gears, fuel tanks, oil tanks, and engine components for military aeronautic industries. Magnaghi Aeronautica Spa has over 200 employees and is headquartered in Naples, Italy.

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Mortenson Construction Implements BIM Process on More Than 100 Projects Including Harley-Davidson Museum

23 July 2009

Autodesk, Inc. has announced that Mortenson Construction, a Minnesota-based firm that provides diversified construction services, has been selected to receive an Autodesk BIM Experience Award.

The firm is being honored for using building information modeling (BIM) on more than 100 projects since 1998 at a total construction value exceeding $6 billion. Mortenson Construction is also being recognized for its use of Autodesk software for BIM, including Autodesk Revit Architecture, Autodesk

Revit Structure and Autodesk Navisworks, on projects ranging from resort hotels to the Harley-Davidson Museum.

"BIM and Autodesk's portfolio of BIM software are a mainstay at Mortenson and are used in every aspect of our construction practices," said Derek Cunz, director of project development, Mortenson Construction. "In fact, we're one of only two pure contractors to be included in *Building Design & Construction* magazine's Top 50 BIM Adopters ranking from their 2009 Giants 300 Report."

BIM Process Solves Harley-Davidson Museum Challenge and Reduces RFIs on Tulalip Resort Hotel Project

The design scheme for the exterior of the 130,000-square-foot Harley-Davidson Museum in Milwaukee, WI, which opened in July 2008, called for exposed components to thematically echo the exposed elements of the historic motorcycles housed in the facility. The key challenge was to balance the scheme for the exterior with the need to minimize visual interference from the complex mechanical, electrical and plumbing (MEP) systems required. To help accomplish the task the team used Revit Architecture, Revit Structure and AutoCAD MEP software as well as a single Autodesk Navisworks 3D model to assist in consolidating and hiding internal structural and MEP elements. The Autodesk Navisworks model (running on a computer in a job-site trailer) was used by foremen, superintendents and subcontractors to plan communicate and review locations in order to help them fit everything correctly.

For the Tulalip Resort Hotel, a $130 million, 12-story, 387-room hotel, spa and conference center in Marysville, WA, that opened in the summer of 2008, the use of a BIM process resulted in a higher level of collaboration with the owner, architect, subcontractors and even onsite craft and trades people. The project team used Autodesk Navisworks software and traditional documentation to create integrated work plans (IWPs). These IWPs were layout drawings given to the field crews that consolidated the construction information for a specific task, combining standard 2D plans and elevations with 3D views from Navisworks software into one delivery source. By using a BIM process, IWPs and a single Autodesk Navisworks 3D model, the team was able to realize a 30 percent reduction in RFIs and a 26 percent increase in production of shear walls. As a result, the team was able to implement a fast-track approach by beginning construction using design documents only 60 percent complete and deliver the project in just 22 months, three months ahead of schedule.

In addition to Revit platform software and Navisworks, Mortenson Construction also uses many other Autodesk software applications to complement its BIM process such as AutoCAD and AutoCAD Civil 3D software. Master Graphics, Madison, WI provides Mortenson Construction with Autodesk software and implementation support.

"A 10-year plus track record implementing and promoting a BIM process makes Mortenson Construction a pioneer in the field of advanced AEC practice," said Jay Bhatt, senior vice president, Autodesk AEC Solutions. "It's no surprise that they received a Technology in Architectural Practice BIM award from the American Institute of Architects in 2003 and 2006, and a honorable mention in 2009. We're delighted to present Mortenson Construction with an Autodesk BIM Experience Award."

The Autodesk BIM Experience Award celebrates professionals and educators around the world who are helping to drive industry transformation through building information modeling. Autodesk honors organizations for their innovation, leadership and excellence in implementing BIM with the help of core BIM products, including one or more of the Autodesk Revit products based on the Revit platform and other Autodesk products that complement the BIM process.

About Mortenson Construction

Mortenson Construction provides diversified construction services, offering customer-centric general contracting, construction management, design-build, program management, project development and "turn-key" development. Mortenson has expertise in a wide range of project types, including healthcare, sports, science and technology, manufacturing, cultural, renewable power, government, hospitality, and corporate. Headquartered in Minnesota, and founded in 1954, Mortenson Construction has over 2,200 employees, operating in 47 U.S. states and China. In 1990, Mortenson Construction reached *Engineering News Record's* list of top 50 contractors, and has remained within the top 50 every year since with a recent jump in position from 38th to 22nd in the publication's July 2009 listing of nationwide, top contractors over the past two years.

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Porsche Selects a PROSTEP Solution

July 2009

Porsche AG in Stuttgart, has selected PROSTEP's OpenDXM® GlobalX as its central data exchange platform.

Quality and reliability are basic requirements at Porsche, not only for its end products but also on the path leading to these products, namely during product development. What the company was looking for was a modern data exchange solution that could satisfy these requirements in addition to a variety of other requirements. An in-depth test phase and final benchmarking involving a number of different portal providers indicated that PROSTEP was best able to meet Porsche's demanding specifications with its OpenDXM® GlobalX data exchange platform. This Internet-based solution enables the secure, stable and standardized exchange of files of any size and type. In addition, the extensive rights management facility offered by OpenDXM® GlobalX allows the access rights to data to be defined for individual groups of people as necessary and, of course, the solutions is also easy for users to work with.

Other requirements dictated that the data exchange solution should be scalable and that it be possible to integrate the solution in the existing infrastructure without investing too much time and effort so that, for example, single sign-on authentication is possible. Another requirement involved easy integration in existing backend systems.

About PROSTEP AG

PROSTEP AG is a leading PLM integration specialist in the area of product data integration. The company offers customers from the aerospace, automotive, shipbuilding and mechanical engineering industries – including EADS/AIRBUS, BMW, Volkswagen, Daimler – integration solutions for CAD, PDM and supplier communication, thus making e-engineering a reality.

The PROSTEP Group has a current headcount of more than 250 in Germany, France and the USA. In addition to its headquarters in Darmstadt, PROSTEP also maintains branch offices in Berlin, Bexbach, Hamburg, Hanover, Munich, Stuttgart, Wolfsburg and Wuppertal, as well as Lyon (France) and Troy, Michigan (USA).

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WorkNC Takes the Problem out of Programming at Expert Tooling & Automation

23 July 2009

Expert Tooling & Automation in the UK is part of the Expert Tooling Group of companies and although it's primary business is with the automotive industry it is thriving despite the current economic downturn. Turnover has grown to £8 million and according to Managing Director, Angelo Luciano, can be attributed to the uniquely broad range of skills the company offers to its customers that few of its competitors can emulate. It is a specialist in producing various tooling and automated special purpose machinery for the production of automotive, machine tool and aerospace products. To guarantee its continued efficiency in its chosen field, the company invested in WorkNC CAM/CAD software to ensure the trouble free machining of its 3D tooling.

One area where Expert Tooling & Automation has been very successful is in the development of interior trim panels for low volume luxury vehicle manufacturers in which complex 3D tooling is required for the accurate location of the veneer laminates prior to bounding onto a substrate, and to also hold the component during the trimming of apertures and excess material. Expert Tooling & Automation has the skills necessary to produce a complete solution for these applications at its Coventry factory. These include designing and machining of its tools and fixtures, specialization in pneumatics to build the clamping and operating mechanisms, and expertise in electronic technology to ensure the overall control and safe operation of the special purpose machines it supplies.

All the tools it produces include 3D shapes, which need to exactly match the surface forms of the panels its customers have designed. WorkNC accepts native CAD data and quickly translates car line designs to the desired machine datum ready for machining. Just one seat of WorkNC keeps Expert Tooling & Automation's six Hurco machines running 24 hours per day. Simon Doleman, Manufacturing Manager, says, "*Our previous CAM system was too cumbersome. WorkNC was recommended to us and, in fact, Rolls-Royce asked us to use it to enable us to share native CAM files.*"

As part of its turnkey service to one particular luxury vehicle manufacturer, the company supplies multi cavity trimming fixtures and the associated 5-axis WorkNC trimming program for finishing the parts on the customer's own machinery. Simon Doleman adds, "*The vacuum fixture we supply contains a complete set of panels for one car, which suits the customized nature of the vehicle and the relatively low volumes. Sescoi worked with us to optimize the 5-axis trimming programs, enabling us to deliver a complete and proven solution to our customer.*"

Expert Tooling & Automation organizes its WorkNC programs to maximize its machine utilization and minimize risk. Programs are written so that roughing operations are completed during the day shift and the long finishing operations overnight and at weekends, when the factory operates on a skeleton staff. Simon Doleman says, "*Roughing is higher risk as tips may need to be changed, while the finishing operations produced by WorkNC never give us any problems. The latter can be successfully run unattended out of normal working hours. Operators already manage more than one machine during the day, so the unmanned working means we achieve nearly 100% machine utilization while eliminating the majority of our labor costs, which makes us very competitive.*"

The efficiency of the cutterpaths produced by WorkNC, the powerful toolpath editing and the tool library are features of the software which Expert Tooling & Automation greatly appreciates. Simon Doleman adds, "*We have set up all the feeds and speeds for hard steel, aluminum and wood, which makes it easy to select the right cutting conditions. We have also noticed that WorkNC produces smooth cutting trajectories with very little wasted movement, and its graphical toolpath editing is fast and efficient and ensures that we are always climb milling. When we visit our customers we sometimes see our competitors tooling. The surface finish on ours is far superior.*"

Since installing WorkNC, programming of toolpaths has become easy and reliable. Simon Doleman

concludes, *"WorkNC is of paramount importance to us and we are very pleased with it. What used to be a source of problems for us has now become a routine exercise, which gives us absolute confidence in the results that WorkNC produces. We are also delighted with the support we get from Sescoi. Their engineers helped us at our customers sites, making sure the 5-axis programs we supplied worked perfectly on their machines."*

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XMOS Uses Magma Talus 1.1 to Improve Quality of Results On New XS1-L1 Event Driven Processor

20 July 2009

Magma® Design Automation Inc. announced that XMOS, a leader in event driven processors™, taped out its recently announced XS1-L1 XCore™ using the Talus® 1.1 IC implementation system. XMOS upgraded to the latest version of the Magma software after early testing showed improvements in the closure of their XCore processor design.

"We benchmarked an early release of Talus 1.1 during the XS1 development program," said Mark Lippett, vice president of engineering at XMOS. "Improvements in the routing algorithms led us to migrate to the Talus 1.1 release for our production tapeout."

The XS1-L family provides embedded software developers with an energy-efficient, scalable, multi-core solution. It enables complete systems that combine interface, DSP and control functions to be built entirely in software. Each XS1-L XCore contains a 32-bit processor and operates up to 400MIPS. XCore power consumption is below 500 microwatts in sleep mode and 20 milliwatts in standby with active power adding under 450 microwatts/MHz. The event-driven architecture, together with XMOS' programming tools, enables XCores to switch automatically between standby and active modes, saving up to 90 percent of energy in low duty-cycle applications. The XS1-L1 is built on a 65-nanometer process. Samples are available now from www.xmos.com.

"Like XMOS, many of our other customers are implementing very complex chips and need a powerful, fast, high-quality chip design system that is also easy to use," said Premal Buch, general manager of Magma's Design Implementation Business Unit. "Talus 1.1 features simplified flows with fewer commands and still provides improved performance, timing closure and power optimization. XMOS' ability to deploy Talus 1.1 quickly to meet their design requirements demonstrates the advantages of Magma's COre technology."

Talus COre Technology

The heart of the improvements in Talus 1.1 is its Concurrent Optimizing Routing Engine (COre) technology. At advanced geometries, complex resistance effects, increased via resistance and crosstalk can create a large timing disconnect between placed gates and final routing. Talus COre focuses on applying the full scope of timing optimization incrementally during routing. Every aspect of the routing algorithms -- from topology generation to layer assignment, track assignment and design rule checking (DRC) violation cleanup -- is timing and crosstalk aware. This allows the design to converge faster and eliminates post-route timing surprises. Talus COre is coupled with Talus' Standard Delay Format (SDF)-based optimization to remove the need for manual engineering change orders (ECOs) to close timing.

About XMOS

XMOS is a leader in event-driven processors for digital electronics. XMOS event-driven processors are high-performance, predictable, processors. They allow complete systems to be implemented in software

using interface, DSP and control code. XMOS is an enabling technology for the Open Source Hardware community. Designs, including USB, Ethernet, and SD-RAM controllers are available in an ever-expanding library of open source code. Free to download, the XMOS development tools are supported by a vibrant community of digital designers and software engineers.

XMOS has corporate offices in Sunnyvale, Calif., Bristol, United Kingdom and Chennai, India and sales offices and representatives across the world.

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Zhejiang Fuchunjiang Hydropower Equipment Co., Ltd Selects Siemens PLM Software's Integrated Solution to Turbocharge Competitive Position

21 July 2009

Siemens PLM Software announced that Zhejiang Fuchunjiang Hydropower Equipment Co., Ltd., (Zhefu) a producer of hydropower equipment, selected an integrated suite of Siemens PLM Software technology to gain competitive advantage.

Zhefu needed a PLM solution to support its strategy to develop hydropower equipment to meet the most demanding requirements both domestically within China's fast-growing market as well as overseas. Zhefu's quest for a PLM solution was driven by the company's need for a more efficient and comprehensive product lifecycle management solution that would help boost its capability to design leading-edge machinery.

Zhefu's comprehensive Siemens PLM Software solution will enable 3D CAD product development, digital design, modeling and product data management through the use of the following products:

NX™ software, an integrated solution for digital product development

NX Nastran® software, a computer-aided engineering (CAE) tool

Solid Edge® software with synchronous technology, the core CAD component of the Velocity Series™ portfolio

Teamcenter® software, a comprehensive digital lifecycle management portfolio

NX, NX Nastran, Teamcenter and Solid Edge provide the mechanical engineering and product information management solutions which will help Zhefu effectively coordinate product-related activities both within the organization and with the company's suppliers and customers.

NX will allow Zhefu to develop 3D digital prototypes for sophisticated hydropower equipment, through powerful modeling and simulation functions. These prototypes can then be tested in a virtual environment by solving analysis problems using NX Nastran. Solid Edge will allow Zhefu to migrate from 2D to 3D design, and Teamcenter will enhance collaboration within the company and with customers across the globe.

"NX, NX Nastran and Solid Edge improve our competitive position in both China's domestic and the global hydropower markets by enabling us to develop superior products and services. For example, we can more quickly create and deliver a component which will fit exactly within the machinery, which is essential for the rapid motion of hydropower equipment. The superior data and resource management capabilities in Teamcenter enhance efficiency and collaboration across the enterprise while boosting overall product lifecycle management. Zhefu selected Siemens PLM Software's product portfolio based

on its proven track record for success in the hydropower industry," said Zhao Zhiqiang, vice president at Zhejiang Fuchunjiang Hydropower Equipment Co.

"Siemens PLM Software solutions are the ideal tools to enable China's hydropower industry to develop leading-edge equipment to meet the country's burgeoning demand for energy. We are pleased that our NX, NX Nastran, Solid Edge and Teamcenter software can help Zhefu realize its strategic objective to advance to the forefront of the global hydropower sector as well as to help meet the country's ambitious plans for greener power generation by efficiently harnessing the country's hydropower resources," said Chuck Yuan, senior vice president and general manager, Greater China, Siemens PLM Software.

About Zhejiang Fuchunjiang Hydropower Equipment Co. Ltd

Zhejiang Fuchunjiang Hydropower Equipment Co. Ltd. (Zhefu) was originally a wholly-owned subsidiary of the Fuchunjiang Hydropower Equipment Headquarters Plant attached to China State Power Co. Ltd. In March 2004, it initiated transformation of the enterprise and in August 2007, became a joint stock limited liability company established by sponsorship. Presently Zhefu is one of China's largest manufacturers of high-tech private large and medium-sized hydropower equipment.

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Product News

BlueCielo Releases InnoCielo Meridian 2009, InnoCielo TeamWork 2009 & InnoCielo Transmittal Management Module

22 July 2009

BlueCielo ECM Solutions announced that it has released InnoCielo Meridian 2009, InnoCielo TeamWork 2009 and the InnoCielo Transmittal Management module. The newest versions of BlueCielo's flagship products include significant changes to provide remote engineering content management capabilities, Oracle's AutoVue 2D Professional embedded as new viewer and enhanced CAD support. BlueCielo is also announcing the introduction of the InnoCielo Transmittal Management module.

The 2009 version of InnoCielo Meridian Enterprise allows users to leverage the engineering content management capabilities of InnoCielo Meridian Enterprise over wide area networks and the Internet. Engineers and subcontractors are no longer restricted by the confines of the local area network and can work from remote locations with engineering content stored in central locations. This new capability also supports scenarios in which InnoCielo Meridian servers are centralized in a global data center.

Oracle's AutoVue 2D Professional is now embedded into the entire InnoCielo suite of ECM solutions. With the introduction of AutoVue 2D Professional, support for hundreds of common file formats including 2D CAD formats such as AutoCAD, MicroStation, SmartSketch, ESRI Shapefile and more, is offered with a single visualization solution, where previously multiple visualizations products were needed to support the most demanding customer environments. This will result in simplified deployment and lower total cost of ownership, in addition to delivering outstanding viewing and markup functionality that will help streamline collaboration across the global enterprise, improve productivity, reduce errors and accelerate time to market. Additionally, an upgrade is available to AutoVue 3D Professional Advanced, supporting all formats supported by AutoVue 2D, in addition to viewing and markup capabilities for 3D CAD formats such as Autodesk Inventor, SolidWorks, Pro/Engineer,

CATIA, Solid Edge and more.

Enhanced CAD support is also now available for Autodesk's AutoCAD 2010 family of products, Autodesk Inventor 2010, AutoCAD P&ID 2009 and SolidWorks 2009, including SolidWorks Virtual Components. This also includes support for the 64-bit versions of AutoCAD, Inventor and SolidWorks.

The new InnoCielo Transmittal Management module is the latest add-on module for InnoCielo Meridian Enterprise. For companies working on complex projects involving third parties, such as customers, subcontractors and suppliers, the InnoCielo Transmittal Management offers full control, tracking and an audit trail of engineering information that is sent and received entirely integrated with the InnoCielo Meridian Enterprise system. This results in projects being executed more efficiently and gaining improved control of projects, budgets and deliverables.

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CAD Schroer Enhances MPDS4 With HOOPS From Tech Soft 3D; 3D Plant Design Software Gains Optimal Graphic Capabilities and Even Wider Platform Support

21 July 2009

CAD Schroer, developers of the MPDS4 product suite, and Tech Soft 3D (TS3D), a leading provider of core graphics components to the engineering software industry, announced that MPDS4, a 3D plant design and 2D/3D factory layout system, is now built with the enhanced capabilities of TS3D's 2D/3D engineering development platform, HOOPS.

"MPDS4 is a plant design and project engineering product suite that offers fast, powerful and flexible large-scale layout, design and assembly capabilities from pre-sales concepts to build order. By including HOOPS within the software we were able to provide significant advantages to our customers. Beyond helping to modernize the interface and graphical capabilities of MPDS4, HOOPS' cross-platform nature enables support on all major platforms, including Windows®, Linux® and Unix®," says Michael Schroer, Founding Director of CAD Schroer.

"Like Tech Soft, CAD Schroer is a company 'by engineers for engineers' so our programmers were extremely pleased to see what CAD Schroer was able to do with HOOPS. We're confident that CAD Schroer customers will enjoy the accelerated graphics capabilities that HOOPS brings to MPDS4," says Ron Fritz, CEO of Tech Soft 3D.

About HOOPS

HOOPS is a high-performance graphics framework used within applications from engineering software companies such as Autodesk, SolidWorks, PTC, MSC.Software, ANSYS/Fluent, COADE, Bentley, Siemens PLM Solutions, Mitutoyo, IronCAD and 200+ others. By leveraging the set of HOOPS libraries, software teams are able to deliver high-performance, visually rich applications to market quickly and cost effectively.

About MPDS4

MPDS4 addresses today's complex industrial engineering design challenges by combining the speed and precision of interactive 3D with the information management capabilities of relational database technology, meaning that the product can handle extremely large assemblies with ease.

MPDS4 offers a suite of multi-user plant engineering applications, including the MPDS4 FACTORY LAYOUT project engineering solution for integrated 2D/3D layout and visualisation.

For more information: http://www.cad-schroer.com/

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KOMPAS-3D now available in Polish and Chinese

20 July 2009

ASCON Group, developer and supplier of CAD/AEC/PLM solutions, announced the official launch of the next version of KOMPAS-3D in Polish and Chinese. Now all the users of the Mechanical Computer-Aided Design solutions for 3D Solid Modelling, 2D Drafting, Design and release of Documentation in these languages will get even easier access to functionalities and abilities of KOMPAS-3D to make their work faster and more effective. Trying to be closer to its customers all over the world KOMPAS solutions from ASCON are now released in 7 languages: English, German, French, Polish, Czech, Chinese and Russian.

Now ASCON is preparing for release of a new, considerably improved and extended version of the MCAD solution – KOMPAS-3D V11, which will include a lot of novelties and enhancements in professional 3D and 2D Design Modellers. These improvements will increase the rate of output and quality of new products, reduce errors in design and as a result help growth of industrial enterprise as a whole.

To download free Demo, LT or Viewer versions of KOMPAS-3D, please, visit ascon.net/download/kompas/

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Lattice Technology Releases Lattice3D Reporter Version 3.0; Application For Interactive 3D In Excel Spreadsheets Now Updated to Support Latest, Most Lightweight XVL Format

21 July 2009

Lattice Technology® announced Version 3.0 of Lattice3D Reporter, the unique application for delivering interactive 3D data in Excel spreadsheets.

Lattice3D Reporter is a sophisticated yet easy-to-use application that delivers interactive 3D product design data in Excel spreadsheets that also contain list data such as work instructions, assembly processes, parts lists, and other manufacturing data. Users can enhance their work performance and productivity by exploiting the interactivity of the data – click on a listed part and the related 3D part will be displayed where it can be viewed, rotated, cross-sectioned, measured and so on. Click on a work process or instruction and the 3D animation related to that process will be shown. Customers using Lattice3D Reporter have experienced significant improvements in assembly processes on the shop floor, parts ordering accuracy and learning of new maintenance processes.

This latest version of Lattice3D Reporter supports the new XVL v10 format, which delivers the industry's most compressed 3D format with no loss of accuracy. XVL v10 can compress 3D CAD data to 0.5% of its original size, allowing anyone in the manufacturing supply chain to quickly view and understand even the most complex 3D CAD data, even on a low specification PC.

Lattice3D Reporter Version 3.0 delivers enhanced tools to more flexibly define 3D animations shown in the spreadsheet, as well as options to show parts paths. Cross-sectioning specific parts from a 3D assembly model is now possible within the spreadsheet, and improved display and buffering options

deliver higher graphics performance.

“Having technical, interactive 3D and list data in a standard format like spreadsheets means that everyone in a manufacturing operation can see, view and understand a product design, work processes, parts lists and BOMs seamlessly,” commented Bill Barnes, General Manager, Lattice Technology. “Productivity improvements for our customers are considerable when they adopt Lattice3D Reporter into their operation.”

Lattice3D Reporter Version 3.0 is available to all maintenance customers now, and can be evaluated via registration at Lattice Technology’s web site at: http://www.lattice3d.com.

Manufacturers can view a demonstration of 3D spreadsheets at: http://www.lattice3d.com/3ddemo/video/Process_Doc/Process_Documentation.html.

More information about the XVL v.10 format is available at: http://www.lattice3d.com/company/tech_3d_image.html.

To understand more about the strategies and techniques for using 3D in a digital manufacturing strategy, Lattice Technology recently released a free downloadable e-book,

‘Improving Lean Manufacturing Through 3D Data’ by Dr. Hiroshi Toriya. The book delivers a series of case studies, survey data and information that help manufacturers understand how to take 3D out of the design stage and make it relevant to a lean manufacturing strategy. This book is available at Lattice Technology’s web site at: http://www.lattice3d.com/book/index_1.html.

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Lattice Technology Releases Updated XVL Converter Products

21 July 2009

Lattice Technology® announced Version 6.0 of its XVL Converter applications, delivering the tools to convert 3D CAD data into the industry’s most lightweight, most accurate 3D XVL format, plus new Converters for 64-bit CAD applications.

The XVL Converter applications are available as both Plug-ins to 3D CAD seats or as stand-alone processors (known as Converter Servers). They accurately convert 3D CAD data into the XVL format, which enables the 3D data to become immediately usable and flexible for downstream uses, and compact enough to be rapidly distributed around a dispersed or global manufacturing operation.

Version 6.0 of the XVL Converter applications supports the new XVL v10 format, which delivers the industry’s most compressed 3D format with no loss of accuracy. XVL v10 can compress 3D CAD data to 0.5% of its original size, allowing anyone in the manufacturing supply chain to quickly view and understand even the most complex 3D CAD data, even on a low specification PC.

These new converters also support the most recent versions of the major 3D CAD applications including:

CATIA® V5 R18 and R19

Pro/ENGINEER® Wildfire® 3 and 4

NX I-deas® 5 and 6

Autodesk Inventor® 2008 and 2009

Mechanical Desktop® 2008 and 2009

CoCreate® 2007 and 2008

Solid Edge® V20 and ST

SolidWorks® 2008 and 2009

NX™ 5 and 6

These latest versions also add more support for 64-bit CAD applications including:

CATIA V5 (64-bit) R18 and R19 (Converter Plug-in and Server)

Pro/ENGINEER (64-bit) Wildfire 3 and 4 (Converter Server)

SolidWorks (64-bit) 2008 and 2009 (Converter Plug-In and Server)

NX (64-bit) 5 and 6 (Converter Server)

In addition, 2 new options for the Converter Servers which support PMI (Product Management Information) data for Pro/ENGINEER and NX have also been introduced.

The new range of Converters are available to all maintenance customers now, and a listing of all supported formats is available at:
http://www.lattice3d.com/products/products_converters_3d_software.html

More information about the XVL v.10 format is available at:
http://www.lattice3d.com/company/tech_3d_image.html

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Magma Announces Support for SMIC Processes With 65-nm Low-Power Reference Flow

20 July 2009

Magma® Design Automation Inc. announced the availability of an advanced low-power IC implementation reference flow for the 65-nanometer (nm) process and low-leakage-process intellectual property (IP) from Semiconductor Manufacturing International Corporation.

SMIC's 65-nm logic technology combines improved performance and reduced power consumption with the increased design possibilities and cost efficiencies that a smaller-node process offers. Magma's Talus® IC implementation system fully supports the SMIC 65-nm low-leakage process intellectual property (IP), including standard-cell libraries, power management kit (PMK) and memory compilers. The Talus implementation flow coupled with Talus Power Pro applies various techniques throughout implementation and to minimize power consumption while maximizing quality of results. Talus reduces turnaround time and the power consumption of ICs used in a wide range of consumer applications, such as mobile phones, personal media players, global positioning, digital television, set-top boxes and mobile storage devices.

"Magma's development of an advanced low-power IC implementation reference flow for the SMIC 65-nm process technology demonstrates both companies' commitment to providing designers with tools and technology to improve performance and reduce power consumption of ICs," said Paul Ouyang, vice president of design services at SMIC.

"Talus is the only flow that enables designers to address power considerations throughout the flow and

within a single environment," said Premal Buch, general manager of Magma's Design Implementation Business Unit. "Using Talus, SMIC customers can get the best combination of performance, low power and fast turnaround times for complex designs."

Availability

The reference flow is available now at no cost to Magma customers.

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Magma Announces Reference Flow for Chartered's Enhanced 65-nm Low-Power Process

21 July 2009

Magma® Design Automation Inc. announced availability of a Talus®-based low-power RTL-to-GDSII integrated circuit design flow for a new enhanced 65-nanometer (nm) low-power process offered by Chartered Semiconductor Manufacturing based on Common Platform technology. The process, called 65nm LPe, utilizes leakage-reduction techniques to significantly improve system-on-chip (SoC) standby power consumption by up to 50 percent.

Based on the Magma Talus IC implementation system, the Chartered 65LPe Low-Power Reference Flow includes Talus Power Pro, which uses various techniques throughout the implementation phase within a single environment to minimize power consumption while maximizing quality of results (QoR) and reducing turnaround time.

This Unified Power Format (UPF)-compliant reference flow was used to implement a complex, hierarchical design incorporating ARM® standard-cell and memory intellectual property (IP) and Aragio Solutions' I/O libraries using a low-power design intent specification and the Chartered 65nm LPe process. The Unified Power Format is a standard supported by a range of EDA suppliers to enable design flows and solutions for low-power design.

"While our customers want low-power solutions, they also want solutions that will help them get to market faster with less risk. Working closely with partners such as Magma, we are able to provide integrated, low-power solutions that enable design teams to meet their project objectives," said Walter Ng, vice president, design enablement alliances at Chartered. "By implementing a complex, hierarchical design, Magma's Talus implementation system proved its ability to maximize the benefits of our enhanced 65-nm low-power process."

"Power consumption has always been a concern for portable and consumer devices, but is now a driving requirement across many application segments," said Premal Buch, general manager of Magma's Design Implementation Business Unit. "We're pleased to support the reference flow for Chartered's 65nm LPe process and to help accelerate the development of next-generation chips that incorporate low-power technology."

Talus Implementation System for Low-Power Designs

The Magma Common Platform 65-nm Low-power Reference Flow is based on the Talus implementation system that includes Talus Design and Talus Vortex, and provides an integrated RTL-to-GDSII flow for high-performance, high-complexity and low-power nanometer designs.

Talus Power Pro works in conjunction with Talus Design, a full-chip synthesis environment, and the Talus Vortex physical design solution to enable optimal power management throughout the flow. It features power-aware synthesis, physical optimization, clock tree synthesis and routing, allowing

designers to minimize power and ensure uniform power distribution.

Talus Power Pro reads in the power constraints from the UPF file at the beginning of the RTL-to-GDSII flow. Power constraints, including power gating, retention-flop synthesis and multi-Vdd domain definitions, can be defined for dynamic power reduction. Special cells such as retention cells can be inferred during the synthesis stage to support multi-Vdd flows. For powered-down domains, switches can be inferred at the register transfer level (RTL) stage to facilitate simulation. State tables can be used to define the relationship between the different domains that have been created. Additionally, Talus Power Pro can write out a UPF file at any point in the design flow for interoperability with third-party tools.

Talus Design is used for the rapid development of RTL and chip-level constraints throughout the design process, and automates datapath synthesis and floorplan generation for prototyping. Talus Vortex is a complete physical implementation system that delivers improved timing and signal integrity, smaller area, lower power, better manufacturability, faster turnaround time and higher capacity than conventional point-tool flows.

Availability

The reference flow is available now at no cost to Magma customers and may be obtained by requesting it from Magma's foundry support team by emailing FoundrySupport@magma-da.com or by contacting a Magma sales representative.

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Magma's Titan Mixed-Signal Platform Supports TSMC's First Interoperable Process Design Kit (iPDK)

22 July 2009

Magma(r) Design Automation Inc. announced that TSMC has qualified Magma's Titan™ mixed-signal platform to support the interoperability and accuracy requirements of the TSMC 65-nm Interoperable Process Design Kit (iPDK). The iPDK eliminates the need to develop and use multiple proprietary PDKs and design databases, enabling full reuse of design data. The combination of Titan's advanced capabilities and the accurate process models and process data provided in the iPDK provides designers with the fastest path to mixed-signal silicon.

Developed through the TSMC Open Innovation Platform™, the iPDK is based on an OpenAccess database and data model. The iPDK features open standard languages, Tcl and Python, for scripting and programming, and includes complete and unified views of symbols, parameterized layout cells, callbacks and technology files. iPDK's modern and flexible architecture easily accommodates specific customizations, future feature extensions and advanced and differentiated development.

"The iPDK allows interoperability across the entire design ecosystem, simplifying design reuse and portability of our customers' mixed-signal designs," said ST Juang, senior director of Design Infrastructure Marketing at TSMC. "Magma has been working with TSMC since last year and has played an important role in validating interoperability and the quality of the iPDK. We're pleased to certify that Titan meets TSMC's high level of iPDK quality standards."

"Innovation in analog and mixed-signal design has been stifled by the lack of predictable design reuse and porting flows," said Anirudh Devgan, general manager of Magma's Custom Design Business Unit. "By working together to validate the iPDK with Titan, Magma and TSMC have removed one of the

most critical barriers to innovation and made it much easier for designers to adopt best-in-class tools such as Titan. When used with the iPDK, Titan will enable designers to accelerate their traditional design flow without any loss of accuracy or performance."

Titan: Fastest Path to Mixed-Signal Silicon

Titan is a unified, open platform that enables integration of digital standard-cell design with analog circuit design. Titan natively supports OpenAccess and emerging industry standards such as the iPDK. The Titan platform offers schematic and layout editors with the full set of features required for full-custom design.

Titan ADX, an integral part of Magma's Titan mixed-signal design platform, focuses on solving analog/mixed-signal design, optimization and porting challenges. Its new, model-based approach allows circuit optimization and porting in a fraction of the time required by traditional simulation-based techniques. Titan ADX takes the guesswork out of analog design, while reducing power and area up to 50 percent. ADX technology enables product groups to push the design envelope for extreme performance, to center the design for multiple process, voltage and temperature (PVT) corner cases, and to reduce power and jitter.

The Titan layout editor provides the fastest access and edit times and the ability to view and modify the digital placed-and-routed data. Coupled with a fast, shape-based analog-aware router, the Titan layout editor gives designers options that range from full custom to full automation to meet specific circuit requirements. These features make Titan an ideal environment for full-custom design as well as chip-level planning, assembly and finishing.

Availability

Magma's Titan mixed-signal design platform will fully support the TSMC 65-nm iPDK starting with its July 2009 release.

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Mentor Graphics Announces Complete Design through Manufacturing Solution in TSMC Reference Flow 10.0

23 July 2009

Mentor Graphics Corporation announced that it has expanded the set of Mentor tools and technologies included in TSMC Reference Flow 10.0. The expanded Mentor® track supports advanced functional verification for complex ICs, netlist-to-GDSII implementation for 28nm ICs, tighter integration with the ubiquitous Calibre® physical verification and DFM platform, and tools for layout aware test failure diagnosis. In addition, this newly introduced Mentor track also addresses low power design with Mentor tools for functional verification, IC implementation and IC testing.

“Mentor Graphics continues to expand its Reference Flow offerings to cover the total IC design cycle from the systems level through functional verification, place-and-route, physical verification and silicon test, as well as offering new solutions such as low power, manufacturing variability, and silicon yield analysis,” said S.T. Juang, senior director of Design Infrastructure Marketing at TSMC.

The Reference Flow 10.0 Mentor track provides new capabilities in many areas, including the first Mentor implementation solution in TSMC Reference Flow, the Olympus-SoC™ place-and-route system. For advanced IC implementation, the Olympus-SoC system has new features addressing on-chip

variation, 28nm routing and low power design:

• **Advanced stage-based OCV analysis and optimization** – Setting different stage-based OCV values helps reduce pessimism and enables faster design closure.

• **N28 routing rules** – Provides 28nm support for the complete netlist-to-GDSII flow, including support for the 28nm transparent half-node.

• **Disjoint power domain** – Supports multiple floor plans in the same voltage domain to minimize congestion and reduce the need for hierarchy changes.

• **UPF hierarchical low power automation** – Provides both top-down and bottom-up support for UPF-based, low-power designs giving designers greater flexibility.

Design-for-Manufacturing capabilities within the Olympus-SoC and Calibre platforms have been expanded and more tightly integrated to address manufacturing variability issues at 28nm and beyond:

• **Litho hotspot fixing** – Improves yield by enabling the Olympus-SoC place-and-route tool to automatically fix litho hotspots detected by the Calibre LFD™ tool.

• **Quick convergence of DMx fill for timing and ECOs** – The Olympus-SoC system invokes the Calibre CMPAnalyzer tool (which works with TSMC's VCMP simulator) to analyze thickness variation for its impact on timing. The Olympus-SoC tool also supports hierarchical, incremental and timing-dr**iven metal fill flows, significantly improving yield and reducing pessimism.**

• **Cell-index-aware placement** – Reduces congestion and speeds routing by allotting more room for cells with difficult pin access.

• **Electrical DFM** – The Calibre xRC™ and Calibre CMPAnalyzer products are integrated to allow simulated thickness information to be incorporated into parasitic extraction results to drive accurate circuit simulation. This also provides a solution for more efficient corner simulation and statistical analysis by providing statistical parasitic information to the Mentor Eldo® circuit simulator.

In addition, the Calibre nmDRC and Calibre nmLVS products support signoff physical verification of 2D and 3D system in package (SIP) designs in Reference Flow 10.0.

Reference Flow 10.0 includes new features in the TestKompress® and YieldAssist™ products for better fault detection, power-aware testing and failure diagnosis:

• **Embedded multiple detect ATPG** – Increases bridge fault detection without any increase in pattern size or test time.

• **Layout aware diagnosis** – Eliminates false bridge/open suspects, enhances diagnosis resolution, and builds a foundation for effective yield analysis.

• **Low-power ATPG** – Reduces power during all phases of scan test utilizing a constant-fill decompressor and power-aware control of existing clock gates.

Reference Flow 10.0 also includes advanced functional verification features from the Questa® and 0-In® platforms for improved validation of complex IC designs.

• Standards-based solution featuring support for IEEE Std. 1801-2009™ UPF and IEEE Std. 1800-2005™ SystemVerilog.

• Integrated low-power simulation and formal capabilities that verify advanced power management circuitry early in the design flow.

• Static and dynamic verification of complex clock domain crossing circuits to ensure proper operation in standard and low power modes.

“The complete Mentor design-to-silicon track in TSMC’s Reference Flow 10.0 allows us to address our mutual customers’ biggest challenges for 28nm, including low power design and verification, large-scale SoC implementation, manufacturing variability, and cost-effective test and yield analysis,” said Walden C. Rhines, chairman and CEO, Mentor Graphics. “The industry transition to 28nm processes also presents new technical challenges, which Mentor is in a unique position to solve. Our close collaboration with TSMC allows us to close the loop between designers and foundries with tools that help our customers get their products to market faster with higher performance and greater reliability.”

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Mentor Graphics Provides Support for TSMC iPDKs

23 July 2009

Mentor Graphics Corporation announced support for the TSMC interoperable process design kit (iPDK) in the Mentor® Custom IC design flow products. This support gives companies using TSMC process technology the freedom to choose best-in-class tools such as the IC Station® tool without the encumbrance of proprietary PDK files, and results in shortened design cycle times and more effective design reuse.

“The TSMC unified iPDK is designed to eliminate the need for multiple proprietary PDKs, and opens the door to greater innovations in custom, analog, mixed-signal and RF design,” said S.T. Juang, senior director of Design Infrastructure Marketing at TSMC. “Support from the EDA community has been outstanding, and we feel the collaborative nature of the work will pay huge dividends to our mutual customers.”

The TSMC iPDK is based on an Open Access database and data model, and features open standard languages for scripting and programming. It includes complete views of symbols, parameterized layout cells, callbacks and technology files. This approach ensures rapid availability of PDKs for advanced technology nodes, and allows TSMC customers more choices of design tools.

“The iPDK initiative is a great example of the industry working together in the best interest of its customers,” said Robert Hum, general manager of Mentor Graphics Deep Submicron Division. “Design kits written in proprietary languages that keep the customer captive to one vendor do not serve the industry well. Interoperability gives a customer the choice and flexibility to buy the EDA tools that best serve their business objectives.”

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Mentor Releases New Calibre Versions Using Interoperable iDRC and iLVS Formats Introduced by TSMC

23 July 2009

Mentor Graphics Corporation announced that its Calibre® nmDRC and nmLVS offerings now support the interoperable iDRC and iLVS formats introduced by TSMC. TSMC and Mentor Graphics collaborated on these vendor-neutral formats for describing physical verification and layout vs. schematic (LVS) checks. The iDRC and iLVS syntaxes make it possible for TSMC and its customers to

create verification decks that will work with Mentor's Calibre nmDRC and nmLVS offerings or other verification products that support the specification. Mentor will optimize the underlying implementation of iDRC/iLVS to deliver optimum performance to end users.

The iDRC and iLVS specifications are based on the open source TCL language extended with specialized functions for verification. It has been validated on the Calibre platform for 40nm designs manufactured at TSMC, and will be rolled out as part of the TSMC reference flow for 28nm designs.

"The TSMC iDRC and iLVS formats benefit both TSMC and its customers by making it possible to define and customize complex verification rules for each of our processes that can in turn drive verification tools from any supporting vendor," said ST Juang, senior director of Design Infrastructure Marketing at TSMC. "This enables us and our customers to easily adapt design rules to new requirements or special situations without worrying about tuning and testing for different tool flows. We've worked closely with Mentor on the architecture and syntax of iDRC and iLVS and have completed first validation on the Calibre tool suite as our lead physical verification platform."

"Our collaboration with TSMC on the definition of iDRC and iLVS helps our mutual customers realize the best possible performance from Calibre products," said Joseph Sawicki, vice president and general manager for the Design-to-Silicon division at Mentor Graphics. "With this collaboration, TSMC ensures their design guidelines are delivered in a consistent manner to all qualified vendors, and Mentor can use its proprietary technology to continue delivering industry-leading verification platforms with the fastest and most efficient underlying code possible."

The Calibre implementation of iDRC and iLVS converts iDRC decks into highly tuned native Calibre SVRF calls for optimum runtime performance. It also includes an interactive TCL debugger with breakpoints and variable monitors integrated with a layout debugger, which is part of the Calibre Results Viewing Environment (RVE), and a special in-line SVRF viewer.

Price and Availability

The Calibre implementation of iDRC is currently being evaluated at selected TSMC and Mentor customer sites. General availability is expected at the end of 2009.

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New Powerful Functionalities for think3's ThinkDesign 2009.1

22 July 2009

Think3 presents ThinkDesign 2009.1, its new release of CAD products developed and enhanced by think3's R&D to offer strong functionality improvements to users in the engineering, styling and tooling departments.

The 2009.1 release includes new features for the creation of frame elements for the industrial machinery market, improvements to commands for curve and surface editing, enhancements in the sheet metal functionalities and many other new features for the Machinery and Components sectors.

Version 2009.1 introduces the new Frame functionality, a fully integrated module of ThinkDesign, which is an instinctive sketch-based method that facilitates the creation of frame elements. The Frame module simplifies the process of creating frame structures with easy-to-use, powerful and flexible tools to achieve significant reduction in design time.

The new Hole command has been redesigned, offering greater ease of use and completeness with respect

to standards, in order to make designer's work increasingly smooth and productive. It can be used for creating and redefining standard, simple, shaped, and free dimensional holes.

The new Mirror mode for curve and surface editing enables the user to maintain continuity of the curve/surface being edited with respect to the virtual mirror of the entity. Additional options under the Mirror mode node give full control to the user to define the type of continuity (Position, Tangent or Smooth curvature) to be maintained about a user-selected plane.

ThinkDesign 2009.1 introduces enhancements in the Global Modeling commands. With the Enhancement in GSM Transformation of Mesh, it is now possible to modify the original mesh thanks to GSM (Global Shape Modeling) technology.

Also new for the Die Design community: the new GSM command called GSM Fillet Reduction. It enables the modification of a set of selected fillet surfaces by changing their curvature, while retaining the desired continuity along borders. It can be used to modify some high curvature areas to let the material fill properly during stamping.

Improvements have been made also in color management to provide better control over the application of colors and increase understanding in complex models (better dynamic visualization). Different colors are now allowed for solid and solid faces, useful to highlight different technological meanings of different parts of the same object. It is possible to use a unique component's color in order to better visualize it in an assembly. Color will be maintained after adding or modifying features and can be maintained after imploding/exploding of solids/surfaces.

The graphic environment has been enhanced with the new 3D Section View mode, the Planar Reflection option in High Quality rendering, the Shaded Drag&Drop for the visualization of components positioned in an assembly in shaded mode, and a set of other features that assist in the visualization of data.

As for new features and improvements in Part Modeling, a new Insert New Faces check box has been introduced in the Extend Faces/Close Solid command selection list which, upon activating, creates new faces to fill the selected holes. It enables an easy closure of holes by saving time in complex models, which is very useful to pre-process shapes used in metal stamping and mold creation.

ThinkDesign 2009.1 includes, among many other features, a completed extension to the CADENAS/PART solutions libraries and the full, seamless integration with TD PLM, think3's web-based solution for implementing a PLM system.

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Pinebush Technologies Delivers HyperPlot for Synopsys Galaxy Custom Designer Solution

23 July 2009

Pinebush Technologies, Inc., provider of HyperPlot™, printing and plotting software for IC design, announced a new solution for printing and plotting tightly integrated into Synopsys, Inc.'s Galaxy Custom Designer™ implementation solution.

Analog and mixed-signal designers require the ability to visualize their designs at larger scales with WYSIWYG fills, stipples and patterns. With HyperPlot's multiple format architecture and the open architecture of Custom Designer, the Synopsys and Pinebush Technologies teams have integrated HyperPlot into Synopsys' custom implementation environment to deliver a best-in-class rasterization solution for Custom Designer users. Utilizing HyperPlot, Custom Designer users can plot to a number of

wide-format plotters, desktop printers, or output to multiple graphics formats, including PDF, JPEG, TIF, and Postscript.

"Our customers require a high-quality printing and plotting solution," said Paul Lo, senior vice president and general manager of the Analog/Mixed-Signal Group at Synopsys. "Pinebush Technologies has been delivering HyperPlot to IC designers for the last two decades and has a strong reputation for the highest performance and breadth of features. At many of our current customers, HyperPlot has long been the standard printing and plotting solution, so integrating it into the Custom Designer environment was an intuitive fit."

"Synopsys has world-class expertise in developing an extensive set of solutions for the semiconductor industry," said George Chandler, president and chief executive officer of Pinebush Technologies. "We believe this collaboration with Synopsys to develop and enhance HyperPlot rasterization capabilities for Custom Designer will be met with strong approval by analog and mixed-signal designers."

About Pinebush Technologies, Inc.

Pinebush Technologies, Inc., headquartered in Albany, New York, is a leading developer of high performance printing and plotting software solutions. HyperPlot has become the standard for plotting in the semiconductor industry with over 35,000 electronic CAD designers worldwide relying on its optimized printing engine. Information about Pinebush and its products can be obtained at http://www.pinebush.com.

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Reveille Management Console for Documentum From Reveille Software Receives Designed for EMC Documentum Accreditation

22 July 2009

Reveille Software announced that its Reveille Management Console for Documentum has received the "Designed for EMC Documentum " accreditation, a mark of quality and value that customers can depend on in enterprise applications. The "Designed for EMC Documentum" accreditation demonstrates that Reveille Management Console for Documentum has successfully met a comprehensive set of criteria for solid design and quality integration.

Reveille Management Console for Documentum integrates with and extends the EMC Documentum enterprise content management platform to provide end-to-end insight of Documentum performance and service levels, and provides real-time monitoring of actual user experience. In addition, the solution monitors critical Documentum components and processes to ensure peak application availability and performance of business-critical content management applications. By proactively monitoring the application, Reveille Management Console for Documentum can automatically diagnose and repair the cause of a problem before users are impacted.

"EMC's position as the leader in enterprise content management is strengthened by the support of great partners such as Reveille Software," said Randy Ziegler, Director of Developer Programs at EMC Corporation. "Partners like Reveille build solutions and applications on the Documentum platform because customers have demonstrated their trust in Documentum to manage their most critical and strategic information. The accreditation program is another way EMC earns that trust while supporting innovative offerings like Reveille Management Console for Documentum."

"Reveille is extremely excited to have Reveille Management Console for Documentum accredited as

'Designed for EMC Documentum'," said Bob Estes, chief executive officer of Reveille. "With Reveille Management Console for Documentum, we provide our customers full instrumentation in an easy-to-implement, packaged solution that provides comprehensive support for managing critical Documentum users and services."

Reveille Management Console for Documentum received design accreditation through participation in the Designed for EMC process which is designed to help ISVs, VSPs and SIs design, develop and go-to-market with successful offerings based on Documentum. As a member, Reveille received specialized design consultation and guidance, along with access to dedicated enterprise content management technical resources. Partners can submit their offerings to be considered for the "Designed for EMC Documentum" accreditation - which if achieved, signifies to customers that the offering meets high standards for architectural compliance with Documentum practices and will provide a reliable integration with less uncertainty for joint customers. To learn more about Reveille Management Console for Documentum and the Designed for EMC program, please visit http://www.emc.com/solutiongallery. To learn more about Reveille Software, visit http://www.reveillesoftware.com.

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Schott Systeme Significantly Reduce CAM Toolpath Calculation Times

23 July 2009

German CAD/CAM developer Schott Systeme GmbH have announced the inclusion of parallel processing functionality within the latest release of their CAD/CAM software 'Pictures by PC 3.4', providing significant reductions of up to 60% in toolpath calculation times.

With machining strategies becoming ever more complex, especially when employing high end 5 axis simultaneous milling and engraving techniques such as those offered by Schott Systeme, toolpath calculation times naturally become longer. However the Schott Systeme team has recently rewritten their software to ensure that the latest 32 and 64 bit versions can parallel process toolpath calculations. By dividing the processing of toolpaths over multiple cores in a computer's CPU, the software has instant access to the extra processing power offered by dual and quad core PC's. Totally transparent to the user, Schott Systeme cite immediate speed gains of between 30-50% for their 32 bit version running on a dual core processor, and anticipate additional gains of up to 60% when running on a quad core. As a result, this is generating immediate savings on every single job machined, without the user having to change the way they work. This compliments Schott Systeme's existing innovation of 'background calculation' enabling users to calculate complex toolpaths while simultaneously working on other parts within a different drawing.

For a demo of some of the latest machining techniques, see http://www.schott-systeme.com/en/new3dmillvideo-en.htm

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Sequence Launches PowerArtist-XP – Industry's First Automatic, Fully Integrated RTL Design For Power Platform

20 July 2009

Sequence Design announced PowerArtist-XP, the first and most comprehensive analysis-driven, automatic RTL power-reduction technology within a completely integrated environment. IP and SoC

RTL designers, without becoming power experts, can analyze, visualize and reduce power by 10-60% or more within minutes on multi-million instances, with 50% fewer RTL edits, and productivity gains of 10X at a minimum.

“Power management is a top priority and Sequence’s PowerArtist-XP is a key tool we use for power efficient RTL design flows,” said Jiebing Wang, Vice President of Acceleration Technology at Exar Corporation. “The tool has provided significant power reduction in our designs. PowerArtist-XP also has enabled our RTL designers to become power aware by providing methods to analyze and reduce power early in the design process while being easy to integrate in our design flows.”

PowerArtist-XP – selected as a DAC 2009 “must-see” by analyst Gary Smith – will be showcased alongside Sequence’s complete technology lineup at this year’s DAC, Booth 3455. For demo and product information: http://www.sequencedesign.com/newsevents/events.php.

The tool delivers maximum power savings, in minimum time, with the least number of RTL edits. Sequence’s new XPRT™ (eXtreme Power Reduction Technology) incorporated here maximizes power savings early at RTL – the highest level of hardware abstraction enabling high productivity. XPRT delivers the industry’s most comprehensive set of RTL power reductions yet – power reduction is not just sequential and combinational clock gating, but is also targeted for memory and datapath portions of complex SoCs and IPs.

Integrating the PowerTheater timing-aware power analysis technology, PowerArtist-XP users now benefit from a one-stop shop for RTL power. By predicting power savings and area trade-offs upfront at RTL, single-pass power reduction identifies the highest impact RTL edits. Productivity increases multi-fold by obviating unnecessary iterations with synthesis and implementation while decreasing the impact on area, timing closure, verification, and functional ECOs. The integrated RTL power environment also enables designers to quickly discover power bugs, manage stimulus for peak and average power, generate custom reports for power regressions using the OpenAccess database, and more.

A graphical cockpit, PowerCanvas™, drives power-ordered reductions while providing a wide range of tightly interlinked visual debug diagnostics that make power easy for mainstream RTL designers. PowerArtist-XP automatically generates power-optimized RTL with surgical changes – in addition, the versatile PowerCanvas reduction dialogs provide both flexibility and precise guidance to the RTL designers in making rapid RTL edits.

“PowerArtist has proven itself by giving us the power savings and productivity gains we need,” said Jon Gibbons, Ubicom Vice President of VLSI Engineering. “By raising the bar with PowerArtist-XP, Sequence continues to advance the state of the art in low-power design, and we look forward to working with this exciting new technology.”

“Since we launched PowerArtist at DAC last year, we saw a growing demand from customers for an integrated solution addressing power reduction more intelligently,” said Vic Kulkarni, President & CEO of Sequence. “For sub-65nm designs, an RTL analysis-driven power reduction approach becomes very critical since surgical changes are now possible in order to achieve maximum possible power reduction with minimal area overhead and minimal ECO loops. Power reduction with analysis-driven vs. ‘blind’ automation is the only meaningful approach for designers to lower power and avoid falling in the traps of poor QoR and an excess of ineffective changes.”

PowerArtist-XP is compatible with all standard design flows, including synthesis, simulation, and formal verification, and all leading formats and constraints including Common Power Format (CPF), Unified Power Format (UPF) and Synopsys Design Constraints (SDC). Utilizing Si2’s OpenAccess

database (OADB), it uniquely allows users to have detailed access to power information to create custom reports or automate proprietary power reductions through an open Tcl API.

Price/Availability

PowerArtist-XP is in production now. North America list pricing starts at $220,000 for a one-year TBL. For more information: http://www.sequencedesign.com.

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SpaceClaim Showcases Multi-Touch for 3D Engineering Design

21 July 2009

SpaceClaim announced the company will enable engineers and industrial designers to leverage Windows Touch to create and edit precise solid models. SpaceClaim marked the news by releasing a highly entertaining and instructive video that demonstrates how multi-touch with SpaceClaim 3D Direct Modeling solutions will impact design and engineering.

Recently, SpaceClaim announced that the company was chosen by Microsoft® as one of a few select Independent Software Vendors (ISV's) in support of the launch of Windows 7 and by N-trig to support DuoSense dual-mode technology, which allows multi-touch in conjunction with a stylus.

"Engineering design represents one of the earliest and most compelling uses of multi-touch technology as it further enhances the ability to employ 3D direct modeling for conceptual design, engineering simulation and analysis, and product styling," said Chris Randles, President and CEO of SpaceClaim. "Touch technology lets anyone create, edit, and visualize 3D models with their fingers. SpaceClaim's software was designed to give engineers and industrial designers the ultimate freedom and flexibility to solve complex design challenges. Our support of multi-touch is another example of our leadership in providing the most innovative 3D Direct Modeling solutions."

Multi-touch – enabling on-screen objects to be manipulated using multiple fingers – is becoming mainstream through the launch of Windows 7 from Microsoft®. While multi-touch is expected to become common on PC hardware, SpaceClaim is ensuring that 3D design will be one of the earliest and most compelling uses of the technology. SpaceClaim will support any multi-touch hardware that uses Windows 7, including those from 3M, N-trig, HP, Dell, and Lenovo.

Windows Touch provides SpaceClaim customers with the most flexibility by augmenting the mouse and keyboard as a new way to interact with solid models.

"Windows 7 reflects Microsoft's commitment to focusing on customers' top priorities and emerging interests," said Mark Rogers, director of Windows Software Ecosystem Product Management at Microsoft Corp. "Therefore, being able to take advantage of Windows Touch technology and the benefits of Windows 7 will help many customers work the way they want and make new things possible. SpaceClaim has worked with us as a valued partner, and its 3D Direct Modeling tools are applications that are ready to utilize the benefits of these new technology breakthroughs."

The engineering benefits of touch in 3D direct modeling include:

• User interface controls are always close to a finger, so less mouse movement is required;

• 3D interaction, such as view panning and rotation, becomes much more intuitive than using a mouse with control keys or requiring separate tools;

• Selection becomes much simpler with conveniences such as select by painting or four-finger box select;

• Modeling becomes more hands-on, so the user experience feels more like working on a real part than a virtual one;

• Real-time, interactive design reviews are enabled by large-format multi touch displays.

SpaceClaim's 3D Direct Modeling solutions include SpaceClaim Engineer and SpaceClaim Style and represent the most significant advancement in 3D engineering in more than 10 years. These direct modelers enable engineers to work in 3D and engage in conceptual design, engineering analysis, and simulation-driven design.

Earlier this year SpaceClaim announced the fourth release of the company's solutions and, marking an aggressive development cycle, recently announced additional new enhancements through Service Packs. Multi-touch technology will be enabled in the next major release of SpaceClaim, which is due later this year.

SpaceClaim Engineer is a fast, simple, and powerful 3D direct modeler for top-down design, 3D layout, conceptual engineering, and model preparation for simulation and analysis. SpaceClaim Engineer pricing starts at $1,995 per seat. SpaceClaim Style brings 3D solid modeling to industrial designers and product stylists, delivering rapid model creation and versatile editing capabilities that accelerate product ideation and ease interaction with customers and the development team. SpaceClaim Style pricing starts at $895 per seat.

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Synopsys and TSMC Jointly Develop Interoperable Process Design Kit (iPDK) and Interoperable Ecosystem

21 July 2009

Synopsys, Inc. announced that Synopsys and TSMC have entered into a comprehensive multi-year agreement to jointly develop, validate, support and distribute interoperable process design kits (iPDKs) that are optimized for TSMC advanced semiconductor processes including the 65-nanometer (nm), 40-nm and 28-nm nodes. The agreement is the culmination of a two-year collaboration to establish an interoperable PDK ecosystem that can accelerate and broaden designer access to new process nodes, promote design reuse and enable greater analog, mixed-signal and RF design innovation. Additionally, TSMC has adopted Synopsys' Galaxy Custom Designer™ implementation solution as its iPDK development and validation platform.

"We are creating new business models and innovations such as iPDK under TSMC's Open Innovation Platform™," said ST Juang, senior director of Design Infrastructure Marketing at TSMC. "Synopsys has a highly skilled and dedicated team with expertise in developing advanced, high-quality interoperable PDKs, and offers the industry's most open custom design platform that supports iPDKs. This collaborative approach will help to more quickly deliver iPDKs to our mutual customers so that they can begin capitalizing on the benefits of an interoperable ecosystem."

Synopsys was lead developer in the collaborative effort to develop and validate a complete TSMC 65-nm iPDK. Working directly with the TSMC PDK development team and other EDA vendors, Synopsys developed an iPDK that supports the analog, mixed-signal and RF flow on multiple EDA vendor tools. Synopsys and TSMC also collaborated on implementing a comprehensive iPDK development and

validation solution based on Custom Designer. TSMC validated its recently-announced 65-nm iPDK to work with Synopsys' custom design solution, including Custom Designer, HSPICE® circuit simulation, CustomSim™ circuit simulation, IC Validator/Hercules™ LVS/DRC and Star-RCXT™ extraction.

"Open standards are the catalyst for accelerating innovation, increasing competition and fostering growth in the electronics industry," said Paul Lo, senior vice president and general manager of the Analog/Mixed-Signal Group at Synopsys. "Synopsys' open-environment custom design platform and interoperable PDK expertise, coupled with TSMC's comprehensive PDK production capability, has enabled us to move the industry forward to realize the benefits of an interoperable custom design ecosystem. This is a major step for the entire semiconductor industry."

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Synopsys Introduces Galaxy Constraint Analyzer to Improve Designer Productivity; Speeds RTL-to-GDSII Turnaround Time Through Look-ahead Constraint Analysis

24 July 2009

Synopsys, Inc. introduced Galaxy™ Constraint Analyzer, a new tool which improves designer productivity through look-ahead constraint analysis technology tuned for the Synopsys Galaxy Implementation Platform. The Galaxy Constraint Analyzer is an intuitive tool that enables designers to assess the correctness and consistency of timing constraints. Correctness and consistency lead to more efficient runtimes in Synopsys' Design Compiler® synthesis and IC Compiler physical implementation tools. The Galaxy Constraint Analyzer features constraint debug capabilities to help designers eliminate long "trial-and-error iterations" during implementation, reducing design cost as a result of more predictable schedules all the way to full-chip signoff.

"Our complex SoC designs have a large number of clocks that require an intricate set of timing constraint definitions," said Hitoshi Sugihara, department manager of the DFM & Digital EDA Technology Development Dept., Design Technology Div., Renesas Technology Corp. "Making sure that our design engineers start with and hand-off a high-quality set of constraint files significantly lowers risk to our design schedules. Using the Galaxy Constraint Analyzer enabled us to find constraint issues that we could not have found otherwise, saving us significant time and effort. We plan to incorporate the Galaxy Constraint Analyzer into our standard design flow that includes Design Compiler and IC Compiler."

The rapid increase in design size and complexity, as well as the widespread reuse of intellectual property (IP) design blocks, has lead to a major increase in the size and complexity of timing constraint specification files. Ensuring high-quality timing constraints is paramount to efficient design implementation, especially during handoffs between teams. Incomplete, inconsistent or conflicting constraints can cause optimization and implementation tools to run ineffectively or to never converge. To address this challenge, the Galaxy Constraint Analyzer tool provides an extensive set of rule checks designed to maximize the efficiency of Design Compiler synthesis and IC Compiler physical implementation. In addition, Galaxy Constraint Analyzer uses technology based on Synopsys' golden PrimeTime® timing engine to ensure correct interpretation and propagation of constraints. This gives designers a signoff-correlated view of the constraints ahead of each step of the design implementation process. Galaxy Constraint Analyzer's ability to deliver comprehensive constraint analysis on 10-million-gate designs in a matter of minutes, combined with a unique set of interactive analysis and debug capabilities, helps designers quickly identify and fix constraint issues within hours versus days.

"Constraint analysis is becoming a crucial step to ensure an efficient design implementation process," said Robert Hoogenstryd, director of marketing for design analysis and signoff at Synopsys. "However, in order for a constraint analysis tool to be effective, it has to interpret and analyze constraint specifications in a manner that is consistent and correlated with signoff. We built the Galaxy Constraint Analyzer using technology based on the PrimeTime golden timing engine to help designers produce the highest quality constraints for the Galaxy Implementation Platform."

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Synopsys Introduces IC Compiler In-Design Rail Analysis to Accelerate Design Closure

20 July 2009

Synopsys, Inc. introduced its In-Design Rail Analysis™ capability to accelerate design closure. Part of Synopsys' IC Compiler in-design ecosystem, In-Design Rail Analysis utilizes embedded PrimeRail analysis and fixing guidance technology to enable designers to perform power network verification throughout physical implementation. By identifying and fixing voltage-drop and electromigration issues earlier in the flow, designers can eliminate costly iterations late in the design process. Working in concert with IC Compiler's Power Network Synthesis (PNS) and In-Design Physical Verification™ capabilities, In-Design Rail Analysis provides designers with a comprehensive solution for both the implementation and verification of power networks.

"Performing rail analysis and fixing within the IC Compiler place-and-route environment will greatly improve our designers' productivity, a significant benefit of Synopsys' Galaxy Implementation Platform," said Hitoshi Sugihara, Department Manager of DFM & Digital EDA Technology Development Department at Renesas Technology Corp. "We worked with Synopsys early in the development of this technology to ensure that it is easy to use, and have confirmed PrimeRail accuracy and correlation with HSPICE and silicon. We plan to standardize on a design methodology that takes advantage of In-Design Rail Analysis."

Traditional approaches to power network design consist of separate implementation and verification steps, often performed by different engineers using many tools and environments in a complex flow. With leading-edge system-on-chip (SoC) designs, this approach often results in multiple iterations between physical implementation and signoff, adding significant risk to project schedules. By eliminating complicated data exchanges and with no new tools to learn, In-Design Rail Analysis helps IC Compiler users ensure the integrity of their power network early and frequently during the physical implementation process, avoiding late-stage surprises close to tapeout. In-Design Rail Analysis works in tandem with IC Compiler's PNS capability to enable designers to efficiently implement, optimize and refine power networks, significantly reducing overdesign. In addition, In-Design Physical Verification helps ensure that power networks are design-rule clean as refinements and fixes are implemented. IC Compiler's ecosystem of PNS, In-Design Rail Analysis and In-Design Physical Verification today offers a fast and comprehensive solution for power network design.

"The charter of our IC Compiler in-design ecosystem is to bring advanced analysis and verification capabilities into the hands of place-and-route engineers," said Antun Domic, senior vice president and general manager, Synopsys Implementation Group. "Complementing our recent introduction of In-Design Physical Verification with IC Validator, In-Design Rail Analysis is the latest innovation aimed at significantly reducing design iterations which can seriously impact time-to-tapeout."

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Synopsys' New DesignWare IP Slashes Power in Datapath Circuits

20 July 2009

Synopsys, Inc. announced the DesignWare® minPower Components, a new IP product that is an integral part of the Synopsys Eclypse™ Low Power Solution. The DesignWare minPower Components reduce power in datapath logic compared to traditional power optimization methods. By using the DesignWare minPower Components, leading wireless, networking and DSP companies achieved power reduction of up to 48 percent in datapath logic (see Table for results).

"Optimizing the power consumption of datapath circuits in mobile applications can significantly extend battery life because these blocks are often on, even in standby mode," said John Koeter, vice president of marketing for the Solutions Group at Synopsys. "Our customers have achieved an additional 7 to 48 percent reduction in power for these circuits."

"As the high speed networking market evolves to support another 10X increase in data rates, power dissipation has become an important issue in the adoption of next-generation technologies," said Jag Bolaria, senior analyst at The Linley Group. "To be competitive, chip manufacturers need to optimize power dissipation in the datapath. Synopsys' DesignWare minPower Components include innovative techniques that address this problem - enabling designers to further reduce power consumption at advanced data rates."

Today's conventional techniques do not address reducing specific power elements such as glitch power in deep logic levels and dynamic power in high-performance datapath pipelines. The DesignWare minPower Components offer unique, power-optimized datapath architectures that enable the DC Ultra™ synthesis tool to automatically generate circuits that suppress switching activity and glitches, reducing both dynamic and leakage power for mobile devices and high-performance applications. Based on the actual switching activities, transition probabilities, available standard cells and analysis of possible configurations, the DesignWare minPower Components architectures are automatically configured by DC Ultra to implement the optimal structure with the lowest power consumption. In addition to the automatically inferable components, the DesignWare minPower Components also include more than 40 components that incorporate low power design techniques such as enhanced clock gating, built-in datapath gating and patented data-tracking pipeline management technology to reduce power consumption.

The DesignWare minPower Components are integrated with the Synopsys Galaxy™ Implementation Platform, which enables significant optimization of a design's total power compared to existing flows. The unique architectures in the DesignWare minPower Components allow high-level datapath structures to be automatically optimized based on power costing and switching activities. Applications with datapath circuits that have a high percentage of active time, such as wireless receivers, audio/video processors, CPUs, media processors, and signal processing blocks for high-performance networking and storage, are ideal candidates for the DesignWare minPower Components.

The table shows the overall improvements in area and power in datapath circuits as recorded from initial customers designing wireless connectivity and high-performance networking applications. While the total chip power reduction achieved with the DesignWare minPower Components will vary, initial customers have reported design power reductions ranging from 2 to 20 percent in tested modes.

Availability

The DesignWare minPower Components are scheduled for general availability in Q3 of calendar year

2009. For more information on the DesignWare minPower Components, please visit: http://www.synopsys.com/IP/DesignWare%20minPower%20Components/Pages/default.aspx. For more information on the Eclypse Low Power Solution, visit: http://synopsys.com/Solutions/EndSolutions/EclypseSolutions/Pages/default.aspx

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Theorem Delivers More Cost Saving Power in New TPM V3

21 July 2009

In the current economic climate Theorem's TPM is a powerful and 'easy to use' means of saving money. It does this through automating data exchange and collaboration processes and optimising the use of computing resource. TPM V3 brings enhancements designed to extend these benefits and further enhance TPM's costs saving effects.

Automating data exchange and optimising computing resources create savings in man hours and tangible financial saving through the avoidance of direct expenditure on computer resources.

Now a new release of TPM, TPM V3 is even more powerful and delivers new administration and management capabilities. TPM V3 now has the capability to accommodate multiple system administrators thereby allowing enhanced control of job scheduling and load sharing through the optional use of user sub groups, each with their own administrator. This development means that the costs saving capability of TPM V3 can now be finely tuned to the precise requirements of individual groups of users.

TPM V3 provides this capability for both local and wide area configurations and this means that multi-site installations can benefit from local and/or centralised administration, offering the opportunity for savings to be made through improved local procedures and through optimised administration and control.

TPM V3 also includes application enhancements providing, additional functionality in its data archiving functions and improved automatic audit trail creation.

Already popular for its cost saving capabilities in aerospace and automotive OEMs and suppliers, TPM V3 promises additional benefits for new and existing users alike.

For further information on how TPM V3 can save you money visit http://www.theoremsolutions.com/products/tpm.htm

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TSMC Reference Flow 10.0 Includes Apache's RedHawk, Totem, and Sentinel Tools

22 July 2009

Apache Design Solutions announced that TSMC Reference Flow 10.0 includes Apache's RedHawk System-on-Chip (SoC) dynamic power, Totem analog/mixed-signal power and noise integrity, and Sentinel chip-package-system co-design solutions. Apache's products were qualified for power and thermal analysis of System-in-Package (SiP) and stacked-die designs with Through Silicon Via (TSV). Also included is substrate noise analysis for SoC and mixed-signal designs. Specifically, Reference Flow 10.0 includes Apache's advanced solutions:

- RedHawk-NX, Chip Power Model (CPM), and PakSi-E for multi-die/SiP power analysis
- Sentinel-TI, Chip Thermal Model (CTM) for die-package thermal co-analysis
- Totem-SE for substrate modeling and full-chip noise coupling analysis

The demands for higher performance and lower system cost are driving the need for advanced packaging technologies such as SiP / 3DIC which require concurrent analysis of multiple die and package. RedHawk-NX has been architected to handle multi-die simulation via CPM model creation and utilization. PakSi-E provides fast and accurate RLCK model of the package for SiP simulation. User can analyze and optimize the global power delivery network with consideration of the die-to-die power coupling noise.

For 45nm process node and below, managing the interaction of chip power and package heat dissipation becomes a critical challenge for system thermal integrity. Specifically, temperature dependent leakage becomes an important component of total chip power. Sentinel-TI with RedHawk generated CTM provides chip-package thermal co-analysis. Users can analyze thermal profile of multiple die and package to ensure the thermal integrity of system.

With increasing integration of digital, analog, and RF contents in SoC, substrate coupling noise between digital logic and precision analog components becomes an important design constraint. Totem-SE provides accurate multi-layer substrate network extraction and full-chip concurrent simulation of digital and analog power/ground/bulk networks. User can analyze the impact of power and substrate noise coupling to help assess the effectiveness of various guard ring structures.

“TSMC and Apache have been collaborating for over six years to meet the deep sub-micron design challenges of mutual customers,” said Tom Quan, deputy director of Design Service Marketing at TSMC. “In Reference Flow 10.0, Apache provides emerging solutions for managing power, thermal, and substrate integrity for SiP/multi-die, SoC, and mixed-signal designs.”

“Our collaboration with TSMC enables us to define practical methodology for emerging power and noise issues,” said Dian Yang, senior vice president of product management at Apache. “This foundry relationship is important for us to deliver a timely solution to help customers meet their latest design challenges such as the upcoming SiP technology.”

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Virage Logic Offers Broadest Portfolio of Embedded Non-Volatile Memory (NVM) Solutions at TSMC

21 July 2009

Virage Logic Corporation announced it offers the broadest portfolio of embedded non-volatile memory (NVM) at TSMC, with fully qualified IP solutions ranging from 250nm down to 65nm. With a comprehensive selection of multi-time programmable (MTP) and few-time programmable (FTP) NVM IP, the AEON® product family addresses the needs of wireless, automotive, analog, power management and security applications. AEON was developed using proven floating-gate technology on a standard CMOS process that requires no additional masks or processing steps. AEON supports densities from 8 to 16k bits and is multiple-time programmable up to 100k cycles.

"We are pleased to maintain a long-standing partnership with Virage Logic because the company's IP solutions support NVM products in a wide range of TSMC CMOS processes down to 65nm," said Dan

Kochpatcharin, deputy director of IP Portfolio Marketing at TSMC. "Our customers benefit by reducing power, area and costs while increasing data security over external EEPROM solutions when utilizing Virage Logic's NVM product offering available for TSMC's processes."

Virage Logic's AEON MTP memory has been shipped in more than one billion integrated circuits (ICs) to date and has been licensed to leading customers including Analog Devices, Linear Technology, Silicon Image, SanDisk, and Avago.

"No other company has a standard CMOS-based embedded NVM offering that provides the number of off-the shelf-configurations or the process node coverage as Virage Logic's NVM portfolio," said Dr. Yankin Tanurhan, vice president and general manager, NVM Solutions, Virage Logic. "AEON has more than 600 different qualified configurations and has been developed and silicon-proven at process nodes ranging from 250nm down to 65nm, with 40nm and below currently in development."

With Virage Logic's wide-ranging product offering, customers have more options for integrating the flexibility of multiple-time programmable NVM into their designs for wireless, analog, power management and security applications. Designers requiring high reliability use the MTP features of Virage Logic's NVM to conduct thorough electrical testing and improve overall IC test coverage and security, and encryption designers use it to make the overall system more robust against attacks.

Providing reliability and performance benefits over external one-time programmable (OTP) solutions, AEON also serves as an enabler for new features and functionality in designs. Wireless ICs with embedded memory reduce power consumption of the NVM by 50% to 80% over external electrically erasable programmable read-only memory (EEPROM).

Full characterization and qualification data for Virage Logic's NVM is available for eligible customers upon request. For specific process availability or to request a silicon characterization report, contact Virage Logic.

Virage Logic will be a featured partner in TSMC's Open Innovation Platform™ booth (#822) at the Design Automation Conference (DAC) being held July 27-30, 2009, at the Moscone Convention Center in San Francisco, California.

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